

USING SMART DUMMY FILL AND SELECTIVE REVERSE ETCHBACK FOR PATTERN DENSITY EQUALIZATION

Brian Lee^{*}, Duane S. Boning^{*}, Dale L. Hetherington⁺, David J. Stein⁺

^{*}Massachusetts Institute of Technology, Cambridge, MA

⁺Sandia National Laboratories, Albuquerque, NM

Executive Summary

The techniques of dummy fill and reverse etchback are often used prior to a chemical mechanical polishing (CMP) process to prevent film pattern density mismatches that lead to post-CMP film thickness variation. In this work, we present a methodology that utilizes both techniques in an intelligent fashion, and shows that both techniques can be used together to create a better balance of pattern densities than each technique can do separately. We introduce the idea of a selective reverse etchback method to lower the pattern density in high density regions, and smart dummy fill to raise pattern densities in low density regions. We then verify the methodology on the STI active area layer of a test mask.

Extended Abstract

The existence of pattern effect in films polished by CMP processes has been well documented [5][6]. Large variations in effective pattern density have been shown to result in significant and undesirable post-polish film thickness variation. To counteract this effect, two methods are typically used to equalize the effective pattern density across the die. The first method is a process step known as reverse etchback, where areas of high density have large portions of the raised areas etched away, lowering the density of the region. The second method is a layout design step known as dummy fill, where the circuit layout is modified by addition of fill structures to raise the density of low density regions.

Before discussing pattern density equalization methods, it is first necessary to define the term "effective pattern density." Neighboring features around a particular point on a layout affect how that point polishes over time. It is essential to weight the neighboring features around a point when calculating the density at that point. In this way, the actual pressure distribution of the CMP polish pad can be taken into account. Ouma [2] defines a single characterization parameter (planarization length) that describes the proper length scale to be used in the calculation of the effective pattern density of a layout layer. The effective density map is produced by first discretizing the layout locally into cells, and then using an elliptical filter to weight the effects of local density appropriately. The effective pattern density map can then be used to predict the post-CMP film thickness profile. In calculation of effective density, it is also essential to take into account the effects of film deposition bias and etchback.

Dummy fill [1][3][4] refers to the addition of features to a layout for the purpose of raising the density of specific regions on the layout. Conventional dummy fill utilizes a single dummy feature arrayed over the original layout, with sections of the array masked off by an exclusion layer. The exact shape, and dimensions of the dummy structures may vary from layout to layout and may depend on the set of design rules for a given layout. Smart dummy fill refers to the implementation of an algorithm that analyzes the original layout pattern density distribution and customizes the fill structures to minimize the resulting effective pattern density distribution. Such analysis can be complicated since the modification of a single dummy structure will affect the effective densities of many surrounding points.

Reverse etchback involves using a second mask to etch back raised areas in the deposited film, lowering the film density. This procedure is normally used only for STI processes, utilizing the underlying nitride layer as an etch stop. Etchback for other layers is difficult since there exists no etch stop layer, thus requiring a timed etch. The etchback mask is typically created by shrinking all features on a given layout by a fixed amount (“etchback bias”). For large features, this results in a removal of a majority of the raised material, and a resulting low density. This may not be desirable if the densities of other regions of the layout are comparably higher. Selective reverse etchback refers to the customization of the etchback mask that results in less material removed than the nominal etchback mask process. This is accomplished by replacement of a large etchback feature with an array of selective etchback cells, or even the complete removal of etchback features in some regions. The goal is to raise the pattern density in regions where dummy fill is not possible (due to the presence of existing features) such that the effective density range throughout the die is minimized. This results in longer polish times due to higher density regions, but better planarity due to an overall lower pattern density range.

The methodology described below assumes the initial existence of an original layout without dummy fill that includes a reverse etchback process step (e.g. the active area layer in an STI process). The methodology used involves the intelligent selection of both a fill structure for use in conventional dummy fill and a reverse etchback structure for use in a modified etchback layout layer. Preliminary density analysis is critical for the intelligent selection of the pattern density equalization structures to achieve minimal pattern density range. Even for the conventional dummy fill approach, where all fill structures have the same density, it is critical to analyze the original layout to determine the optimal density for the fill structure.

Methodology - The preliminary pattern density analysis can be achieved by generation of an effective density map and profile of the original layout, taking into account the effects of film deposition bias and the etchback process step (one such generation method is described by Ouma [2]). Next, based on the statistics of the density map, select a target density for a dummy fill structure cell. One simple strategy is to select the maximum density that appears in the effective density map of the original layout. However, it is necessary to take into consideration the location and characteristics of the high density regions of the layout. Adding dummy fill to a layout, even if the fill structure density is below the maximum density of the original layout, may modify the maximum density of the dummy-filled layout under certain circumstances. This is demonstrated, but not explicitly stated, in [1], where an original layout with a maximum density of 60% actually resulting in maximum densities of 70% and 80% when conventionally filled with structures of 30% and 50%, respectively.

After choosing the target density, the next step is the construction of a dummy fill cell structure. The exact shape and size of the fill structure depends on the etchback layout bias (if etchback is used), the film deposition bias, and the characteristics of the layout. A smaller cell size will allow for the inclusion of more full dummy structures throughout the layout. Once the dummy fill cell is designed, an array of such cells is then created, of the same size as the original layout. The next step is the creation of a dummy cell exclusion layer, which is generated using the original layout. The exclusion layer is generated using design rules and describes regions on the layout where dummy cells cannot be located (due to proximity to existing features, overlap with other layers in the design, or other such restrictions). This exclusion layer is then used to mask off dummy structures (and portions of dummy structures) from the dummy cell array. The modified array is then merged with the original layout.

Next, the original layout effective density map is inspected for low density regions that are due to large reverse etchback regions. These are typically large features in a layout (such as a large capacitor) that would nominally evaluate to 100% density without the etchback, but evaluate to very low density as a result of the etchback. A reverse etchback cell is then created, using the same target density as was used for

the dummy fill structure. When creating such a cell, one must take into account that the etchback layer is typically an inverse image (i.e. drawn features are the features that are etched). Thus, if the target density was 25%, the etchback cell would have a drawn density of 75%. This would leave a desired post-etchback raised area density of 25%. Arrays of the selective reverse etchback cells are then used to replace large reverse etchback features on the original reverse etchback mask. Figure 1 shows a comparison of conventional and selective reverse etchback features.

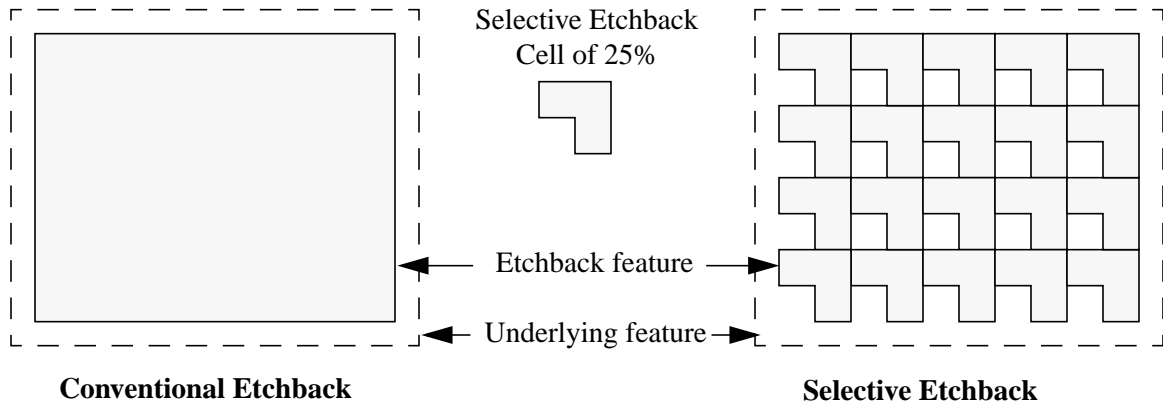


Figure 1: A comparison of conventional reverse etchback and selective etchback features

The result of the above steps will be a modified layout and etchback layout for the original layer of interest, with a significant reduction in the effective pattern density range. The modified layout density distribution can be verified using the aforementioned effective density calculation methods.

Verification - The STI layer of a test mask was used to verify the methodology. The 14 mm x 14 mm layout contained test structures and a 256K SRAM circuit. This STI process utilizes etchback with an original etchback layer produced with an etchback bias of 0.5 μm . A film deposition bias of 0.3 μm was used. Localized pattern density information was created using a density extraction tool from PDF Solutions, Inc., using a local discretization distance of 40 μm . Effective pattern density maps were generated according to the methodology described by Ouma [2], using an elliptical weighting function with a planarization length of 3.5 mm. The fill structure was determined by using the maximum density present in the original layout.

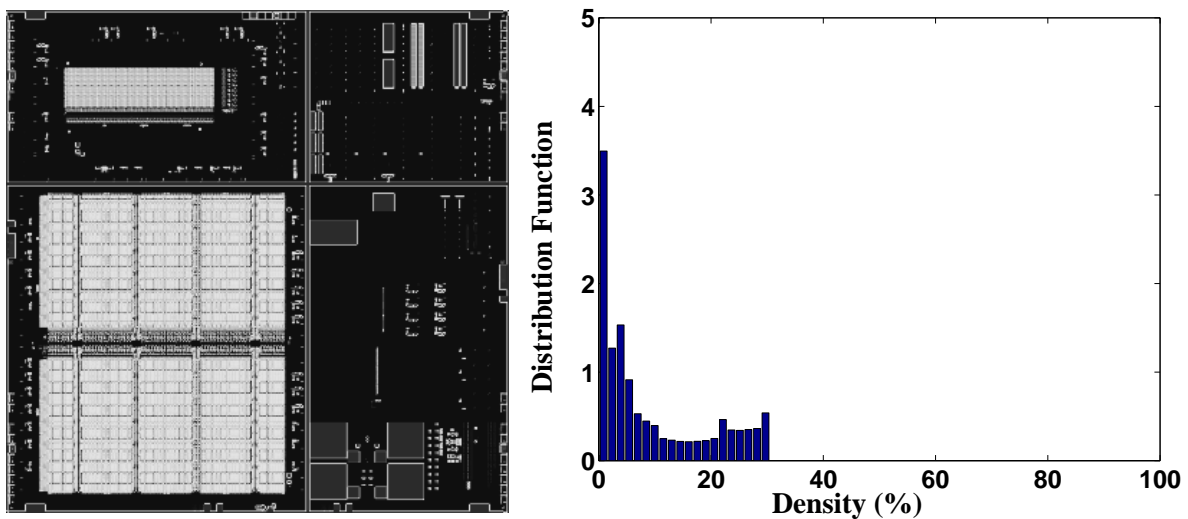


Figure 2: Test mask layout and original density distribution

Table 1 shows the simulated effects of various fill structures on the resulting density variation of the test layout. As can be seen, the variation is minimized using a fill structure of 30% density, while using a 50% density fill structure results in significantly smaller reduction of the density range. The last row of Table 1 shows the additional density variation benefits from using a selective etchback approach in addition to optimal dummy fill.

Table 1: Density variation results for various fill structures

Test Case	Density Variation (%)	Max	Min	Mean
Original Layout (with conventional etchback)	30.36	30.46	0.10	9.20
Fill (10%), conventional etchback	18.49	26.46	7.97	13.86
Fill (50%), conventional etchback	28.18	47.83	19.65	35.65
Fill (30%), conventional etchback	17.90	32.14	14.24	25.79
Fill (30%), <i>selective etchback</i>	14.40	31.36	16.96	26.05

These results show that the methodology may be used to effectively reduce the amount of density variation in a layout by a significant amount. Incorporation of this methodology offers a comprehensive and analytical way of minimizing the post-CMP film thickness of arbitrary layouts for STI and dielectric CMP processes.

Acknowledgments

The authors much appreciate the help of PDF Solutions, Inc., for the use of their density analysis tool. The authors also would like to thank Mike Oliver (Rodel Inc.) and Rob Jarecki (Sandia National Laboratories) for discussions and useful suggestions.

References

- [1] G. Liu *et al.*, "Chip-Level CMP Modeling and Smart Dummy Fill for HDP and Conformal CVD Films," *Proc. CMP-MIC Conf.*, February 1999, pp. 120-127.
- [2] D. Ouma, *Modeling of Chemical Mechanical Polishing for Dielectric Planarization*, *Ph.D. Thesis*, MIT, November 1998, Chapter 5.
- [3] S. Sun *et al.*, "Active Layer Mask with Dummy Pattern," *US Patent #5,902752*. May 11, 1999.
- [4] E. Nowak *et al.*, "Pattern filled photo mask generation for integrated circuit manufacturing," *US Patent #5,597668*. January 28, 1997.
- [5] P. Burke, "Semi-empirical modeling of SiO₂ chemical-mechanical polishing planarization," *Proc. VMIC Conf.*, 1991, pp. 379-384.
- [6] E. Chang *et al.*, "Using a Statistical Metrology Framework to Identify Systematic and Random Sources of Die- and Wafer-level ILD Thickness Variation in CMP Processes," *IEDM Technical Digest*, 1995, pp. 499-502.