ADVANCED PROCESS CONTROL IN DIELECTRIC CHEMICAL MECHANICAL POLISHING (CMP)

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Abstract

The decrease in device dimensions is placing extremely tight constraints on many aspects of the CMP process. We outline four key areas that will provide significant steps toward attaining this level of control. In particular, we discuss the need for improved in-line surface topography metrology, and show that that high resolution profilometry appears to meet this need. We demonstrate the need for new metrics to monitor and control CMP planarity, and present evidence which suggests current methods of step height measurement are insufficient for this task. The use of *in-situ* sensors and on-line metrology is shown to provide significant improvement in our ability to monitor and control post-CMP film thickness. The use of *in-situ* sensors in compensating for incoming thickness variation is outlined. Finally, the use of on-line metrology for accurate monitoring and control of specific locations is shown.

I. Introduction

As device dimensions continue to scale down, chemical mechanical polishing (CMP) is becoming more and more critical in the process flow. Scaling of the device dimension not only puts stringent restrictions on the CMP process, but also on CMP metrology requirements, process development, process monitoring, and process control. The purpose of this paper is to discuss how each of these areas will be affected by tightening specifications on and new problems in the CMP process. Section II will begin by outlining how a new topography metrology tool will enable monitoring and control of new and old problems in the CMP process. Section III will then discuss some common misconceptions about standard metrics used in process development. In particular, we will show that the common definitions and metrics of planarity are insufficient for characterizing the CMP process. In addition, we suggest possible alternatives that will enable us to meet future demands on post-polish surface topography. We will then outline CMP metrology requirements for advanced film thickness control, including both *in-situ* and on-line metrology, in Sections IV and V. In particular, Section IV will discuss on-line CMP metrology, and the opportunity it creates for effective use of advanced process control. Section V will outline the characteristics of *in-situ* sensors and their use for CMP endpoint detection. Finally, conclusions will be provided in Section VI.

II. Characterization of Surface Topography

Current trends in process technology are moving toward smaller devices, which are requiring extremely tight control of post-CMP topography. This is driving the need for higher quality surface topography metrology in CMP. As shown in Figure 1, hillock formation in metal films creates a possibility for faults to occur during CMP. In this case, the metal hillock can cause unwanted exposure of the low-k material during CMP. Since some low-k materials have high

etch rates in a dilute HF solution, the unwanted exposure of low-k material will lead to a very high defect count after CMP. As a result, characterization of small geometry features, such as metal hillocks, becomes important to CMP process development and integration. The need to monitor minute surface topography effects places a new requirement on CMP metrology.

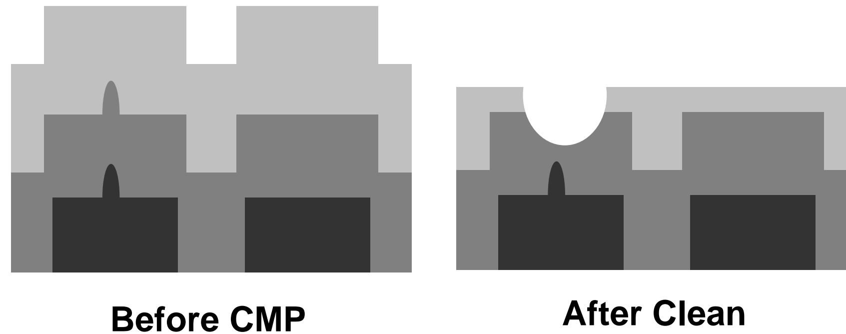

Figure 1. Hillock formation in metal film, and the defect resulting from CMP and cleaning. Note that low-k material is deposited on top of metal, and the cap oxide is then the deposited on top of the low-k material. The metal hillock can cause an unwanted exposure of low-k material during CMP, leading to a post-CMP defect.

Conventionally, we use profilometry to measure large features, and cross section scanning electron microscopy (SEM) or atomic force microscopy (AFM) to measure small features. Recently, high resolution profilometry (HRP) has been utilized to characterize post-CMP topography.[1] HRP can provide non-destructive 3D images (see Figure 2). HRP is less time-consuming than SEM, so it can be used as an in-line technique to characterize the post-CMP topography. Figure 3 shows the correlation of the "dishing" measured by SEM and HRP. The high correlation suggests that HRP can provide an in-line alternative to SEM for the characterization of post-CMP topography. More importantly, HRP can measure geometry that is typically measured by AFM. However, current commercial AFM cannot measure features larger than 100µm.[1] This restricts AFM from providing information on erosion and other long-range CMP effects. Combing the capabilities of micro- and macro-scans, as well as lower measurement times, HRP is highly qualified to provide in-line characterization of post-CMP topography, such as via recess, field oxide dishing, and via array erosion.

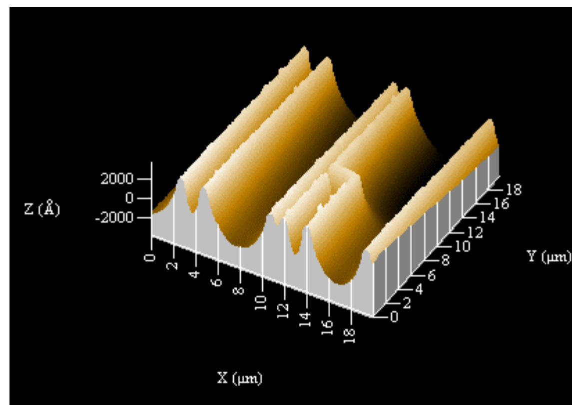

Figure 2. A 3D image characterized by high resolution profilometry.

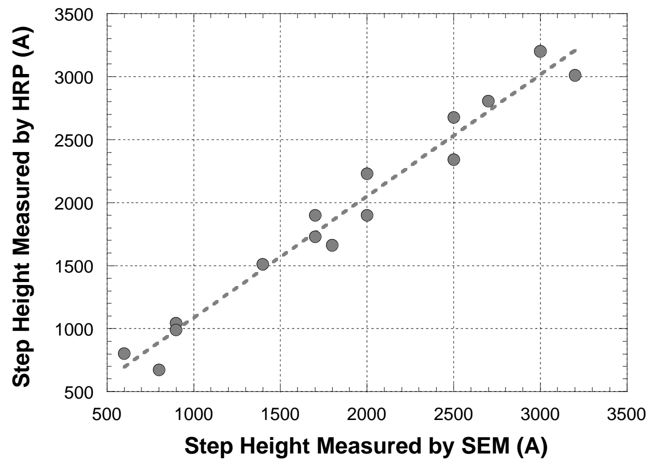

Figure 3. Correlation of step height measured by HRP and cross section SEM.

Metrology such HRP outline an important element to the future of process development and control in CMP. In particular, the monitoring and control post-polish CMP surface topography, including dishing, erosion, and potential surface defects, will help to meet future requirements for post-CMP topography.

III. CMP Process Development

The goal of CMP is to reduce the topography on a wafer, and achieve global planarization. However, the definition of planarity is an ambiguous one. If the step height of certain features (e.g. bond pads) is below a certain level, then planarity is achieved, is a typical requirement for process engineers. This is often coupled with measurements of multiple similar features on multiple dies. Other works have suggested that longer range "steps", or thickness variations, exist.[2-5] In this section, we would like to consider the impact of one definition versus another, as well as how our choice will affect our ability to meet the increasing need for highly planar post-polish surfaces.

We begin by considering how process development is done today. Typically, process engineers first develop a CMP process on unpatterned wafers in order to optimize the within wafer non-uniformity (WIWNU). In order to determine the effectiveness of the process on patterned wafers, step height is then measured on a typically random feature, in order to determine when planarity is reached. Since step height reduction is correlated to the amount of material removed, process engineers then determine the pre-CMP deposition thickness target based on step height measurements. Figure 4 illustrates the step height of two different locations within a die, as a function of oxide removal. As seen in Figure 4(a), the three processes reach the planarity at the same removal target. However, Figure 4(b) shows that process C has a much better planarity than the other two processes. This implies that we will reach a different conclusion, depending on the choice of the measurement location. This suggests that step height measurement is not a very good measure of planarity. It only provides us with information about local planarity, rather than the planarity within a whole die or within the whole wafer.

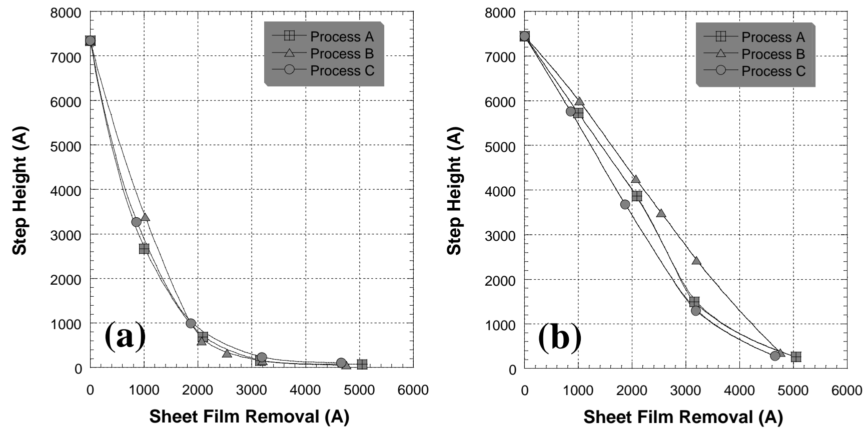

Figure 4. Step height reduction of three different CMP processes. A low density area is shown in (a), and a high density area in (b).

Other works suggest global planarity is more closely associated with the within die non-uniformity (WIDNU).[2-5] Figure 5 shows the range (i.e., the difference between max and min) of 25 measurement sites within a die, as a function of oxide removal. As seen in Figure 5, the three processes lead to different WIDNUs. All three of these processes have given us nearly identical WIWNU. However, we can greatly improve the WIDNU by changing the polishing parameters (i.e., speed and pressure) and the consumable set. WIDNU may be a good measure to characterize a CMP process. However, WIDNU is not a universal parameter because it is strongly dependent on the choice of measurement locations and on the device layout. Recently, the use of a standard mask to characterize the CMP process has been proposed by the MIT.[2-3] We can extract a simple parameter, planarization length, from an MIT test mask to assess a CMP process. In general, the higher the planarization length, the better the process is. In this experiment, the planarization lengths of process B and C are 4.0mm and 5.3mm, respectively. The trend in planarization length is similar to that of WIDNU (see Figure 5).

Another means for improving WIDNU is shown in Figure 5. Here we see that the within die range first increases as oxide is removed, but then decreases as polishing proceeds. The range of the pre-polished film is very low (~500Å). As polishing proceeds, the increase in the range at the beginning of polishing is due to the CMP pattern density effect.[2-4] Previous CMP models proposed that the polish rate of patterned wafers is the same as that of the un-patterned wafers when "planarity" is reached. This implies that we cannot improve the WIDNU after the planarity is reached. Based on the step height measurements shown in Figure 4, "planarity" should be reached after 6000 Å of oxide removal. As seen in Figure 5, the WIDNU significantly improves by removing more oxide. A detailed analysis to extend the current CMP model will be provided elsewhere.[6] This further serves to illustrate that step height measurements are not good indicators of planarity, because using the step height measurement in Figure 4(a) does not indicate that continuing to polish would improve performance. A better definition of planarity is needed to incorporate this spatial information. Planarization length is perhaps a better method to describe within-die planarity because it includes spatial information on planarity.[2-3]

Most of the work on CMP process development in the literature focuses on the effect of polishing conditions and consumable sets to improve WIWNU. In fact, WIDNU has far more

implications on the non-uniformity of device characteristics. For example, a high WIDNU of the interlayer dielectric (ILD) thickness will cause a high variation in the aspect ratio of vias. Without dummy structures to reduce the CMP pattern density effect, the range within a die can be as high as 3000-5000Å (see Figure 5). This number is much larger than the range within the un-patterned wafer (<1000Å). As a result, the WIDNU consumes more depth of focus budget in the lithography step than does the WIWNU. Therefore, achieving a higher level of planarity in CMP for future device dimension reductions will require us to move away from traditional step height measurements. These lithography requirements will drive the need for new definitions and metrics for planarity, such as WIDNU or planarization length.

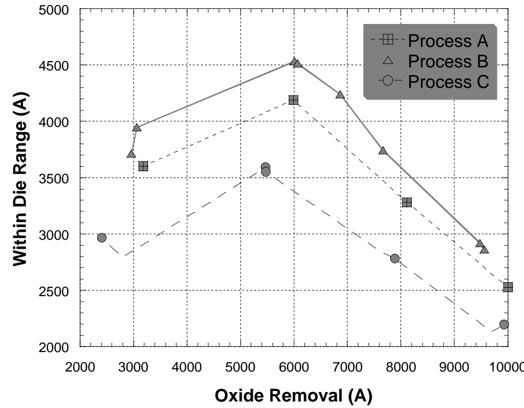

Figure 5. Within die range vs. oxide removal for three CMP processes.

IV. Thickness Control Using *In-Situ* Sensors

Due to process variations such as pad lifetime, slurry chemistry, film properties, and pattern densities, process engineers rely on extensive *ex-situ* metrology to monitor and control the CMP process. The lack of a polish stop layer for backend dielectric CMP processes results in a wide range of variation in the post-polish ILD thickness. Recently, *in-situ* (i.e. endpoint)[7-10] sensors and on-line[11-12] metrology that monitor the CMP process have been reported. The *in-situ* technologies reported in the literature include measurement of optical, electrical and thermal signals.

Table1 summarizes the capabilities of *in-situ* sensors and on-line metrology. Both *in-situ* sensors and on-line metrology can serve as a partial replacement for *ex-situ* metrology. With *in-situ* sensors or on-line metrology, a removal rate drift can be corrected before the test wafer is cleaned and measured by *ex-situ* metrology. Since the cleaning and *ex-situ* metrology steps are very time-consuming, it is not possible to frequently monitor the removal rate variation in a manufacturing environment. The utilization of *in-situ* sensors and on-line metrology not only improves CMP throughput and cost, but also improves yield and creates a more robust manufacturing process. These factors will make the use of these technologies in advanced process control systems critical for meeting the demands of improved CMP performance.

Unlike on-line metrology, current *in-situ* sensors are designed to provide real time process control, and can correct for incoming thickness variation (i.e., the variation due to film deposition). Current *in-situ* sensors are based on indirect measurements. Specifically, a significant amount of development is required to correlate the signals with the physical thickness

on a wafer. Thus, the development of a control algorithm for CMP is not straightforward for *in-situ* sensors. More importantly, some *in-situ* technologies are not only sensitive to the thickness or topography of a wafer, but also to other CMP process variations. This leads to poor repeatability in endpoint signals.[8] In addition, the setup of an endpoint algorithm can be very empirical in nature because of the lack of understanding in the endpoint signals. In some cases, design rules (i.e. trench depth, oxide thickness, feature size, and feature density) must be changed in order to setup an endpoint algorithm. Figure 6 shows three optical endpoint traces of an STI CMP process.[7] Trace (a) and (b) represent two identical devices (Device A), except trace (b) uses a reverse-moat etch. As seen in Figure 6, the reverse-moat etch changes the oxide thickness at the moat, leading to a significant change in the endpoint trace. Trace (c) represents another device (Device B) with a reverse-moat etch. The difference between device A and B is the trench depth (or oxide thickness within the trench). As shown in Figure 6(c), we are not able to setup an endpoint algorithm using trace (c) because of a lack of a peak or a valley within the trace. Consequently, we will have to modify the design rules (i.e., change either the STI thickness or the trench depth) in order to have a peak (or valley) within the signal. In general, the endpoint traces are sensitive to small changes in the design rules. Consequently, it is very difficult to setup a single endpoint algorithm to handle multiple devices.

	In-Situ	**On-Line**
Throughput Improvement	Yes	Yes
Real Time Control	Yes	No
Correct Pre-CMP Thickness Variation	Yes	No
Pattern Recognition	No	Yes
Accurate Thickness Reading	No	Yes
Inert to Process Variations	No	Yes
Inert to Design Rule	No	Yes

Table1. Comparison between *in-situ* sensors and on-line metrology.

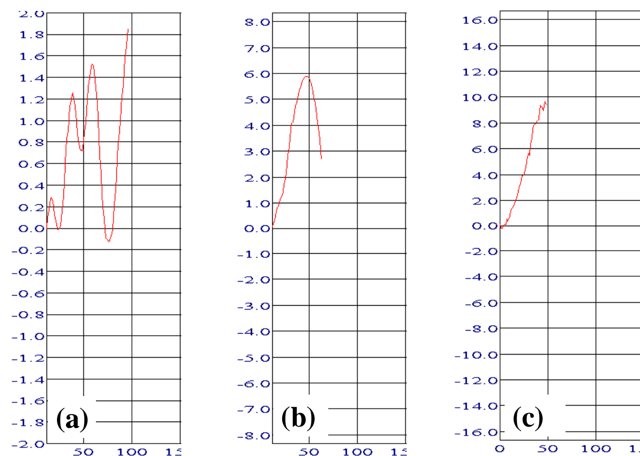

Figure 6. STI endpoint traces (i.e., optical signal vs. time). Device A w/o reverse-moat etch is shown in (a). Device A with reverse-moat etch is shown in (b). Device B with reverse-moat etch is shown in (c).

V. Thickness Control Using On-Line Metrology

In general, current endpoint technologies are indirect measurements and can only provide information about the overall thickness or topography change within a wafer, rather than accurate thickness measurements of particular sites. Unlike *in-situ* technologies, on-line metrology can provide accurate thickness readings of particular measurement locations.[11] Figure 7 illustrates a comparison of on-line and *ex-situ* measurements. As seen in Figure 7, thicknesses measured by on-line and *ex-situ* metrology tools correlate very well with each other. The standard deviation of the spread is only 12 Å; far less than the accuracy required for CMP.

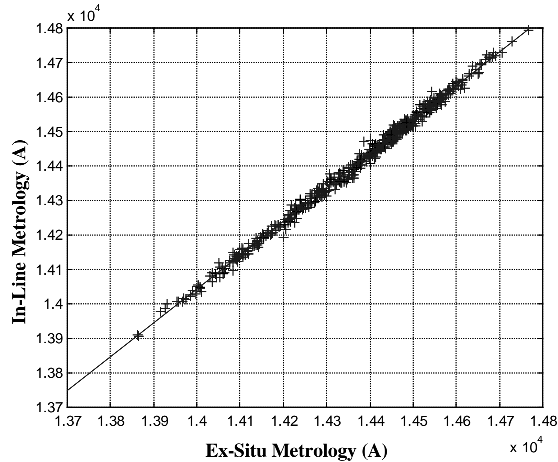

Figure 7. Correlation of on-line and *ex-situ* metrology measurements. Both technologies are based on spectral-photometry. Note that the average spread is 12 Å, and the offset is 47 Å.

Since the on-line sensor has been proven to be accurate and reliable, it may be used for CMP run-to-run control.[12-13] Figure 8 shows the post-CMP thickness variation of a 600-wafer run-to-run control experiment. The exponentially weighted moving average (EWMA) controller was used to adjust the polishing time, and the results indicate that the on-line metrology tool is robust in its use for controlling the CMP process.[12] One drawback with on-line technology is that it cannot easily correct for incoming thickness variation. To do so, we must perform pre-polish thickness measurements (see Table1).

The ability to monitor and control the CMP process using *in-situ* sensors and on-line metrology is rapidly becoming a means for meeting the future demands for improved post-polish film thickness control. However, significant effort is needed by process engineers to determine the polishing time for changing devices. Typically, we have to estimate the polishing time for the unknown device. Since the polishing characteristics for patterned wafer are very non-linear, it is difficult to accurately estimate the polishing time. Current focus is to incorporate a CMP pattern independent model into the control algorithm. Results which describe this model based process control strategy will be discussed later.[14]

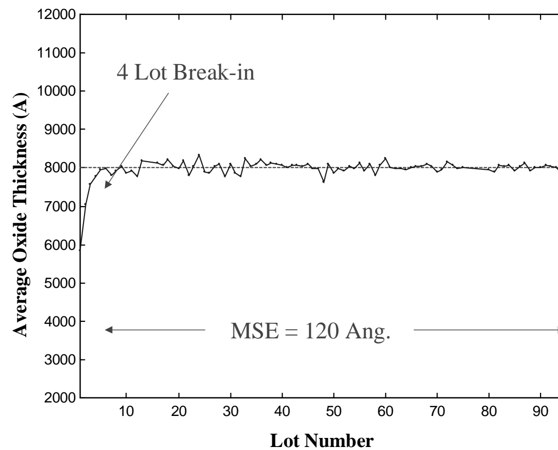

Figure 8. Results on the run-to-run control experiment. Mean standard error is only 120 Å for more than 90 ILD patterned wafer lots.

VI. Conclusions and Future Work

We have outlined the need for advanced surface topography metrology, such as high resolution profilometry, to increase our ability to meet future demands of CMP wafer quality. These demands also require improved metrics for characterizing, monitoring, and controlling post-polish planarity. We have shown experimental data that demonstrates current methods of step height measurement are insufficient for this. Finally, we have demonstrated that recent developments in *in-situ* sensors and on-line metrology are creating opportunities to significantly improve post-CMP thickness control. This includes the use of *in-situ* film thickness sensors to account for incoming thickness variation, as well as accurate monitoring and control of post-polish thicknesses at specific locations using on-line metrology. These four advances in CMP monitoring and control technology will provide a means for significantly improving post-CMP wafer quality.

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