ELECTRICAL CHARACTERIZATION OF COPPER CHEMICAL MECHANICAL POLISHING

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ABSTRACT

In this work, we present an electrical characterization methodology targeted at studying the pattern dependent problems of metal dishing and oxide erosion in inlaid metal polishing processes [1]. The method includes electrical test structure design and layout, design of experiment and measurement, physical thickness extraction procedures, and verification with physical measurement. The electrical test structure design and layout is focused on the generation and mask floor planning of test structures to capture each pattern dependency without being confounded with other patterns or structures. This study uses a newly developed electrical test mask targeted at studying these pattern dependencies not only physically but also electrically by taking line resistance measurements. The key e-test structure used in this study is a modified Kelvin structure which makes up different pattern structures. The methodology includes carefully designed statistically meaningful experiments and relevant metrology procedures. The physical thickness extraction procedure, which is the heart of the proposed methodology, converts electrical line resistance measurements to physical copper thickness. The verification of extracted copper thicknesses is done using profilometry scans and SEM cross sections to correlate to physical thicknesses. The data shown for extracted thickness versus physical thickness indicate a good correlation, and demonstrate the effectiveness of the electrical characterization approach.

I. INTRODUCTION

Copper metallization is emerging as the next generation interconnect technology as the feature size decreases to the deep sub-micron regime. Unlike traditional metallization of aluminum, where aluminum is deposited on top of inter-level dielectric (ILD), patterned, and etched, copper metallization requires a damascene process because copper is hard to etch. In the damascene process, ILD is first deposited and patterned to define “trenches” where the metal lines will lie. Then, metal is deposited to fill the patterned oxide trenches and polished to remove the excess metal outside the desired lines using chemical-mechanical polishing (CMP). Ideally, the polished copper should be perfectly flat; unfortunately, an important non-ideality is that copper lines suffer from dishing and erosion due to CMP. Figure 1 shows a cross sectional view of the ideal case and a comparison to a realistic case suffering from dishing and erosion. Dishing is defined as the recessed height of a copper line compared to the neighboring oxide, and erosion is defined as the difference between the original oxide height and the post-polish oxide height.

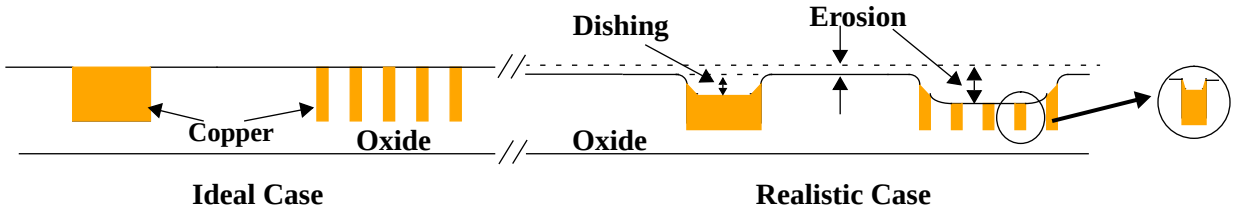


Figure 1. Pattern Dependent Problems of Dishing and Erosion

These structure pattern and polish time dependent problems of copper dishing and oxide erosion are major challenges in advanced copper metallization processes. Such problems affect the manufacturability and performance of a chip by reducing the remaining copper thicknesses in various regions of the chip which cause a variable increase in copper line resistance. An increasing number of papers are being pub-

lished on these physical thickness variations [2, 3, 4, 5], but only a small number have examined electrical characterization and have considered only resistance and sheet resistance without any further extraction to physical thickness [4, 6]. In this work, we present electrical characterization in addition to physical characterization to fully understand planarization and electrical behaviors in copper metallization processes.

II. OVERVIEW OF CHARACTERIZATION METHODOLOGY

To characterize in-laid metal polishing behaviors electrically, a methodology is developed that builds upon a statistical metrology framework for oxide polishing [7]. The method includes test structure design and layout, design of experiment and measurement, physical thickness extraction procedures, and verification with physical measurement.

The electrical test structure design and layout is focused on the generation and mask floor planning of test structures to capture each pattern dependency without being confounded with other patterns or structures. This study uses a newly developed electrical test mask targeted at studying these pattern dependencies not only physically but also electrically by taking line resistance measurements. The ability of electrical test is especially good for studying fine geometry features, gathering large amounts of data, and obtaining yield data. The design of experiment and measurement is concerned with carefully designed statistically meaningful experiments and relevant metrology procedures. The physical thickness extraction procedure, which is the heart of this methodology, converts electrical line resistance measurements to physical copper thickness. This procedure uses geometrical parameters of the feature of study to obtain remaining copper thickness as a function of measured line resistance. The validity of this extraction procedure and the obtained thickness is done by correlating the extracted copper thicknesses to profilometry scans and SEM cross sections.

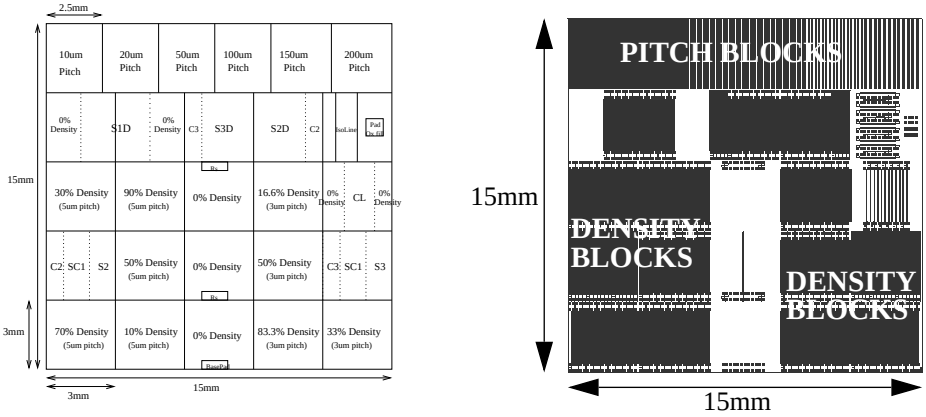
In the following sections, we will describe in detail the test structure and mask design, measurement and extraction procedures, and show results for a time split experiment with the electrical characterization mask. The experiment in this work is carried out at SEMATECH using a short flow process. The process consists of deposition of 3000 Å oxide on 8" Si wafers, 1000 Å Si_3N_4, followed by 7000 Å TEOS, patterning and etching TEOS down to Si_3N_4 layer, deposition of 250 Å barrier layer, and deposition of 1000 Å PVD Cu seed layer, and 1.5 μm electroplated Cu. Wafers are then polished with a fixed process and consumable set for different time splits (e.g. different amounts of overpolish). The polished wafers are measured using HRP (high resolution profilometer) for surface scans, and using an optical measurement tool for oxide thickness in field regions. Then, they are electrically tested using HP4062 to obtain line resistance values, and SEM is done to verify extracted copper thickness and physical data.

III. MASK DESIGN ISSUES AND DESCRIPTION

A newly designed electrical test mask is specifically targeted and optimized to examine pattern dependency in inlaid copper polishing, and can be also used for yield and defect analysis. In the overall mask floor planning as well as test structure design, the most crucial design factor is estimating the interaction distance for the copper damascene CMP process. Each test structure (e.g. pitch and density structures) is to be designed with a large enough size so that any interactions from neighboring structures can be excluded. In oxide CMP, the interaction distance is found to be between 3mm and 5mm for most conventional polish processes and pads [8], and industrial feedback and speculation indicated that the interaction distance in copper polish may be considerably less than that of oxide polish. Thus, a structure size of 3mm x 3mm for the density structures is chosen, which should be large enough to allow decoupling of specific density dependency between structures. A slightly smaller block size, 2.5mm x 3mm, for the pitch structures is chosen since all pitch structures have fixed density of 50% and because the dishing within pitch structures is assumed to be minimally influenced by neighboring structures (dishing within features occurs at much shorter length scales than the interaction distance).

The layout of the copper damascene mask is shown in Figure 2. The mask is mainly composed of 3mm x 3mm blocks for the density structures, and 2.5mm x 3.0mm blocks for the pitch structures. In this mask design, pitch is defined as line width plus line space, and metal density is defined as the ratio of line width to pitch. Metal density, still maintaining the same definition, can also be thought of as the ratio of an area of copper within a given region to the total area of that region. In this study, "metal density" refers to the designed metal density within any test structure region with corrected line width and line space from SEM cross sections. In addition to density and pitch patterns, the mask also includes electrical serpentine and

comb test structures to characterize electrical yield for minimum feature (0.35μm line width and line space) and other fine metal lines. There are also other structures, which are not described in this study, such as control lines, oxide filled pads, and Van der Pauw structures.



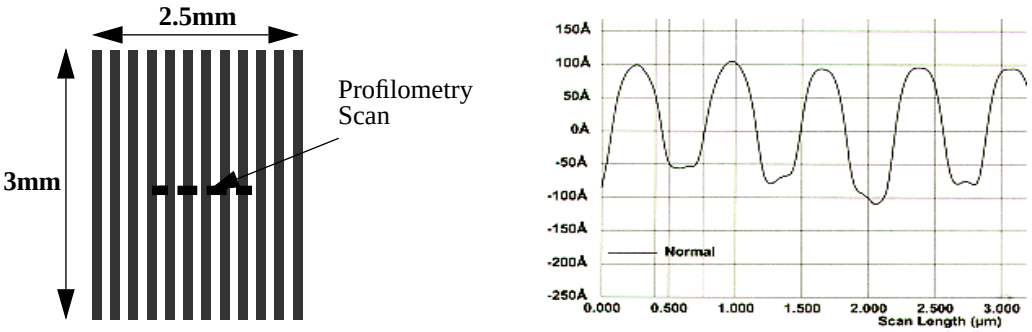
a. Mask Floor Plan **b. Mask Layout**

Figure 2. Electrical Test Mask

The characterization mask utilizes only a single layer; there is no separate mask for bond pads. Although the single layer mask provides simplified processing, the approach has the potential to perturb the local density near test structures. However, the single layer mask does provide the necessary structures for extensive evaluation of dishing and erosion effects and any pad influence can be accounted for during the analysis.

IV. PITCH STRUCTURE: PHYSICAL

In the pitch structures, pitch values range from 10μm to 200μm as shown in the top row of Figure 2 with the fixed local density of 50%. The block size for each pitch structure is 2.5mm x 3mm, and each structure consists of vertical lines 3mm long as shown in Figure 3a. Large pitch values are chosen for easy profilometry and optical measurements (in between copper lines). These structures are used to characterize pitch dependencies: dishing vs. pitch and erosion vs. pitch.



a. One Sample Pitch Block **b. Sample Dishing Scan (0.35μm line width and line space)**

Figure 3. One Block of the Pitch Structure and Measurement Method

A short profilometry scan across a few copper lines in the center of each structure is made to measure dishing, and a sample scan is shown in Figure 3b. Dishing should be measured as the height difference from the oxide (right next to copper line) to the bottom of a dished copper line. This measurement is repeated for all pitch structures and also for 50% density structures which also serve as pitch structures.

Optical measurement is performed over oxide in the middle of each pitch structure to obtain oxide erosion. Figure 4 shows dependence of dishing and erosion on polish time and pitch values extracted using these structures and physical measurements.

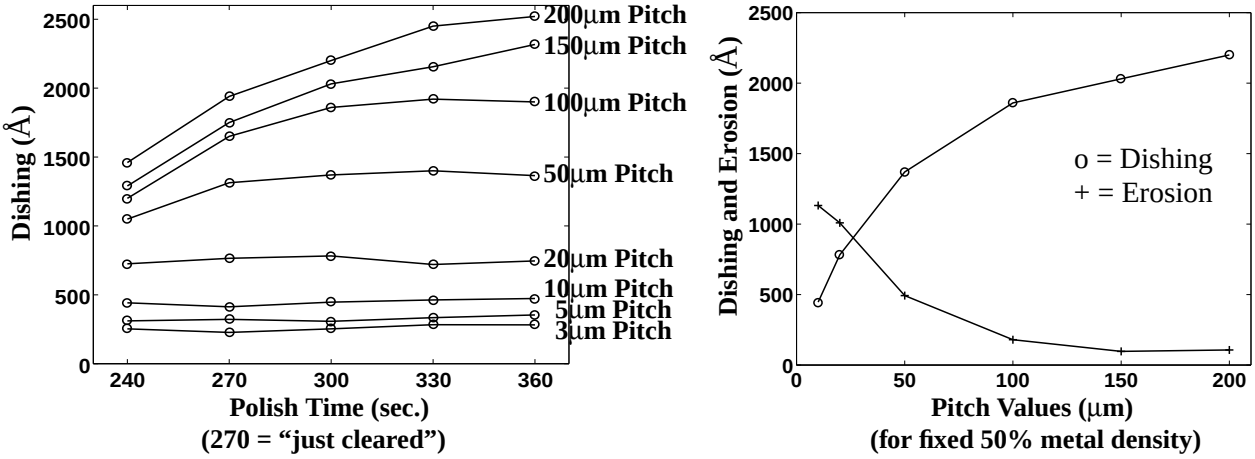
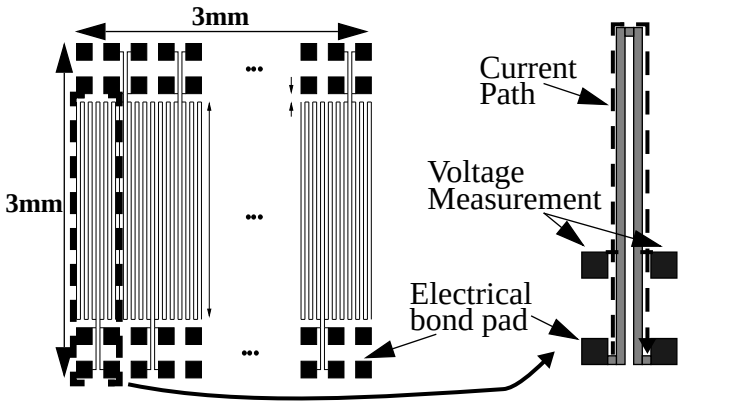


Figure 4. Dishing and Erosion Dependencies on Polish Time and Pitch

TABLE 1. Line widths and Line spaces in Density Structures (units in μm)

3μm Pitch (line width/ line space/ density (%))	5μm Pitch (line width/ line space/ density (%))
2.5/0.5/83.3%	4.5/0.5/90%
1.5/1.5/50%	3.5/1.5/70%
1.0/2.0/33%	2.5/2.5/50%
0.5/2.5/16.6%	1.5/3.5/30%
	0.5/4.5/10%



a. Density Structure **b. Modified Kelvin Structure**
(neighboring serp. lines are not shown)

Figure 5. Electrical Structure Design and Layout

V. DENSITY STRUCTURES: PHYSICAL AND ELECTRICAL

In the density structures, density is varied for fixed pitch values of 3μm and 5μm. In the mask layout of Figure 2, one column of blank oxide (0% density) regions is surrounded by other density structures ranging from 10% to 90% density to determine the interaction range and its possible dependence on density. The density structures are also placed so that there are notable differences in density between adjacent structures. Figure 5a shows one 3mm x 3mm density block structure, and Table 1 shows the line widths and line spaces used for 3μm and 5μm pitch value structures. The key e-test structure used in the density structures is a modified Kelvin structure which makes up different pattern structures by altering line widths and line spaces as shown in Figure 5b. Note that the density structures are implemented with serpentine style lines. Thus, metal lines bend around at the top and bottom so that measurement can be made from either bottom or top pads (the use of both top and bottom pads is to increase the number of measurements that can be made on each structure). Serpentine lines also allow simultaneous resistance measurement on one loop of a line or array of lines for thickness extraction and continuity test of lines in the density structures.

The electrical measurement is done across a large array of serpentine lines which spans from one edge to about 2/3 of a structure. A surface profilometry scan is done to obtain erosion and dishing on those structures. The erosion profile is measured from the initial oxide level to the bottom of the recessed region in each density block. Optical measurements are also made to determine the absolute remaining oxide thickness in the field region since surface profiles only give relative height and to correct any leveling problems.

A. COPPER THICKNESS EXTRACTION PROCEDURE

A data conversion procedure enables the extraction of remaining copper thickness from electrically measured line resistance. After line resistances are obtained, they are converted to copper thicknesses for further analysis. The copper thickness extraction method is based on the following equation:

$$R = Rs \times \frac{L}{W} \qquad \text{or by re-arranging variables} \qquad T = \frac{\rho}{R} \times \frac{L}{W} \qquad \text{(Eq. 1)}$$

where R is resistance, Rs (ρ/T) is sheet resistance, T is the thickness of a line, ρ is the resistivity of copper, L is the length of a line, and W is the width of a line.

In this equation, ρ and L are assumed to be constant, but W suffers from linewidth variations during lithography and etch processes. This linewidth variation must be accounted for to obtain the correct copper thickness from the line resistance measurement. Since it is hard to extract correct line width from electrical measurements due to both thickness and line width variation, we use direct physical measurement by SEM cross section to obtain the exact line width. Ideally, the linewidth estimation measurements should be made at different locations within a structure (e.g. density structure) to account for within-structure variation. However, it is expected that all the regularly laid out vertical lines except those within about 20μm of the edge of the structure will have a similar amount of line width variation. In this study, lines near the center of each structure are measured to obtain the correct line width.

To be more accurate in the copper thickness extraction method, the impact of barrier liner should be accounted for. Equation 1 assumes the ideal case where the effect of liner is assumed negligible. However, as the critical dimension decreases to the sub-micron regime, the thickness of liner consumes a higher percentage of the width of the line and the total thickness of metal. For the purpose of this study, we assume a constant liner thickness and a simplified dishing characteristic (i.e. a flat surface in the dished copper line and no edge rounding) as shown in Figure 6.

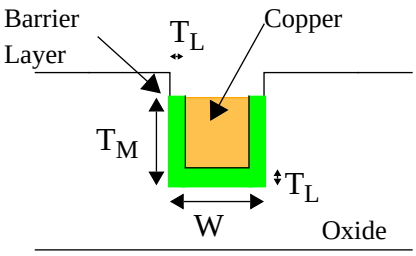


Figure 6. Simplified Profile

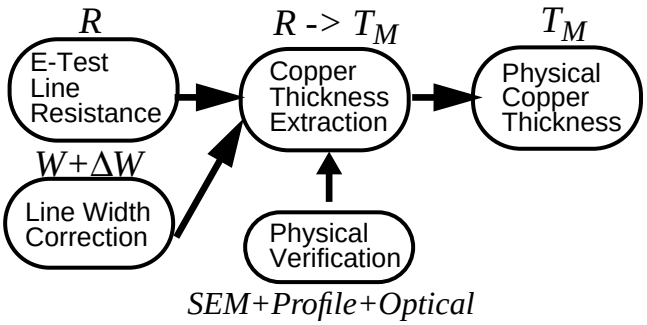


Figure 7. Copper Thickness Extraction Procedure

First, we examine R_{Cu} and R_L (resistance due to copper and due to liner) and represent them as

$$R_{Cu} = \frac{\rho_{Cu} \times L}{(T_M - T_L) \times (W - 2T_L)} \qquad \text{and} \qquad R_L = \frac{\rho_L \times L}{(2T_M \times T_L) + ((W - 2T_L) \times T_L)} \qquad \text{(Eq. 2)}$$

where ρ_{Cu} is the resistivity of copper, ρ_L is the resistivity of liner, T_M is the remaining metal thickness, and T_L is the thickness of liner. The denominator terms in both equations give the cross sectional area. The resistivity of commonly used barrier liners are in the range of 50 to 100 μΩ-cm. We assume the worst case scenario where ρ_L is 100 μΩ-cm and W is 0.35μm (minimum linewidth in the mask design). We also

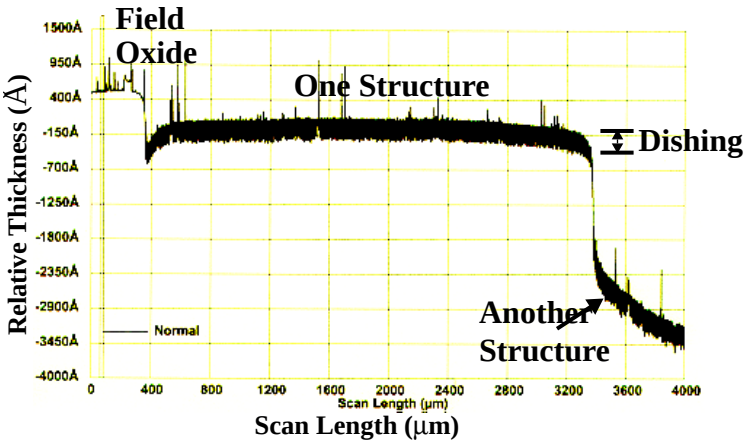
assume that T_M is about 4000 Å (half of the ideal trench height in this experiment) and T_L is 250 Å. By using these numbers in the equations above, the ratio of R_L to R_{Cu} is calculated to be about 200. This indicates that the copper and liner stack can be approximated just as a copper line with less than 0.5% error. Thus, Equation 1 can be rewritten to account for the liner effect as (i.e. by using R_{Cu} rather than $R_L \parallel R_{Cu}$)

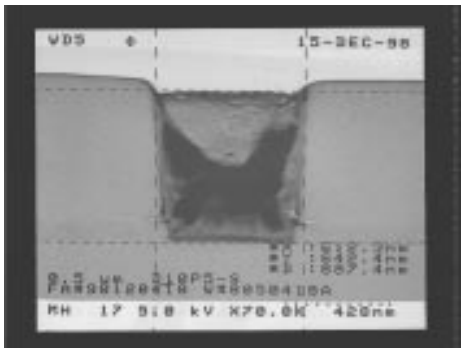
$$T_M = \frac{\rho_{Cu}}{R} \times \frac{L}{(W - 2T_L)} + T_L \qquad \text{(Eq. 3)}$$

T_L is added to get the total thickness of copper plus the liner. The overall extraction procedure is shown in Figure 7.

B. EXTRACTION RESULT AND DISCUSSION

Figure 8 shows a sample surface scan from oxide field region to one density region to another abutting density region and a SEM picture. Figure 9 shows copper line resistances and sheet resistance variation across different density structures from one time split wafer (300 sec. polish or 11% overpolish). Without dishing or erosion, the raw resistance of copper lines should decrease with higher metal density structure because the linewidth is increasing (with fixed line length). On the contrary, Figure 9 clearly indicates that line thickness loss occurs at high densities. This non-ideal behavior is better seen with the sheet resistance data. The R_S increases with higher metal density values due to higher erosion on the high density structures. The extracted copper thickness from these electrical data is shown in Figure 10 for polish times of 270, 300, and 330 seconds. Also shown in Figure 11 is the extracted and physical thickness as a function of polish times, indicating good correlation between the extracted and physical thicknesses.





SEM Cross Section
(0.5μm wide line)

Figure 8. Sample Erosion Profile and SEM Picture

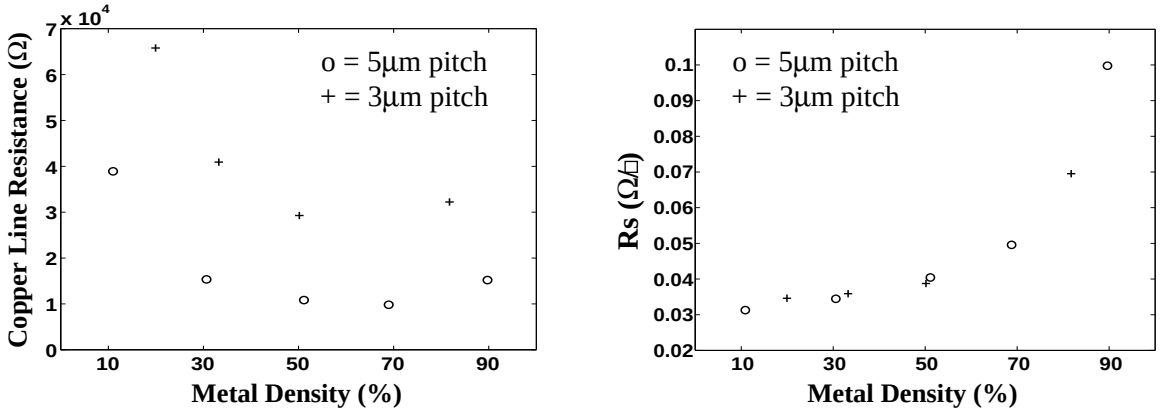


Figure 9. Raw electrical line resistance and sheet resistance variation due to thickness variation (data shown for 300 sec. polish)

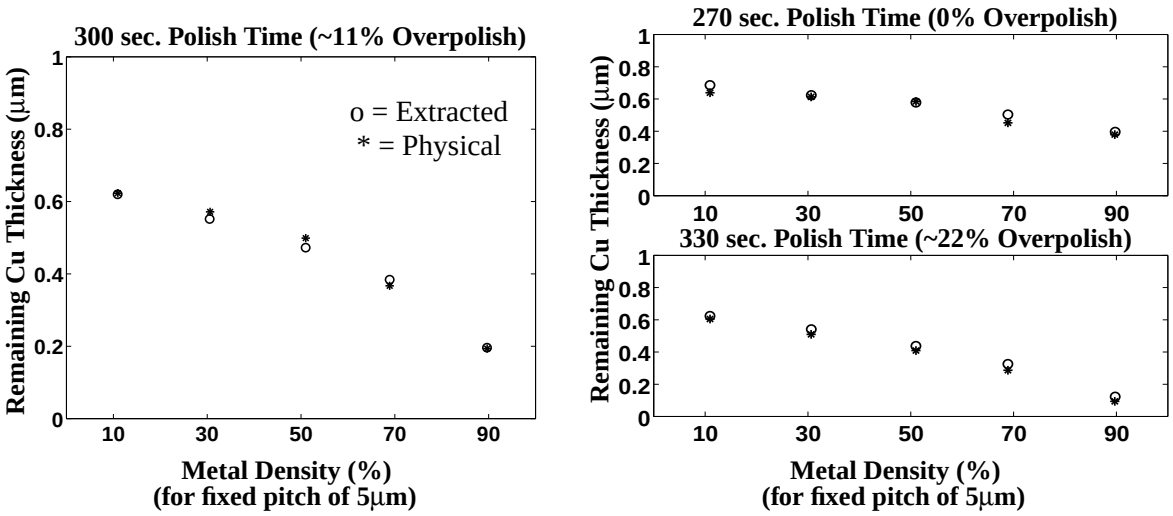


Figure 10. Extracted and Physical Copper Thickness.

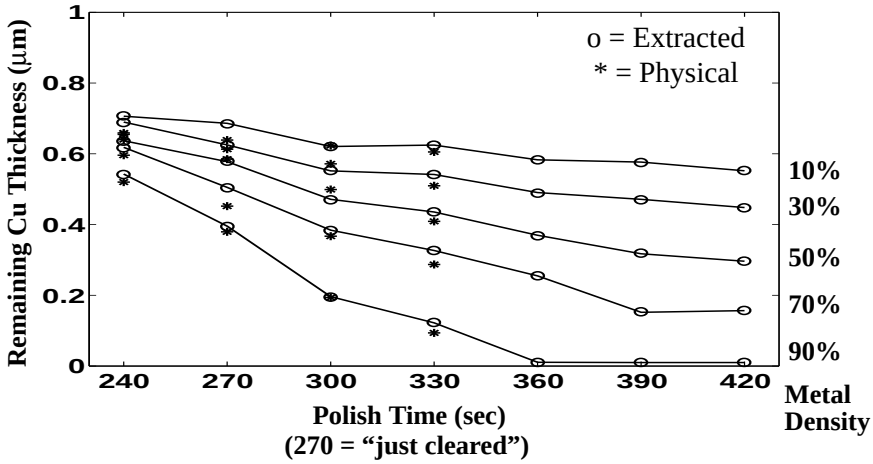
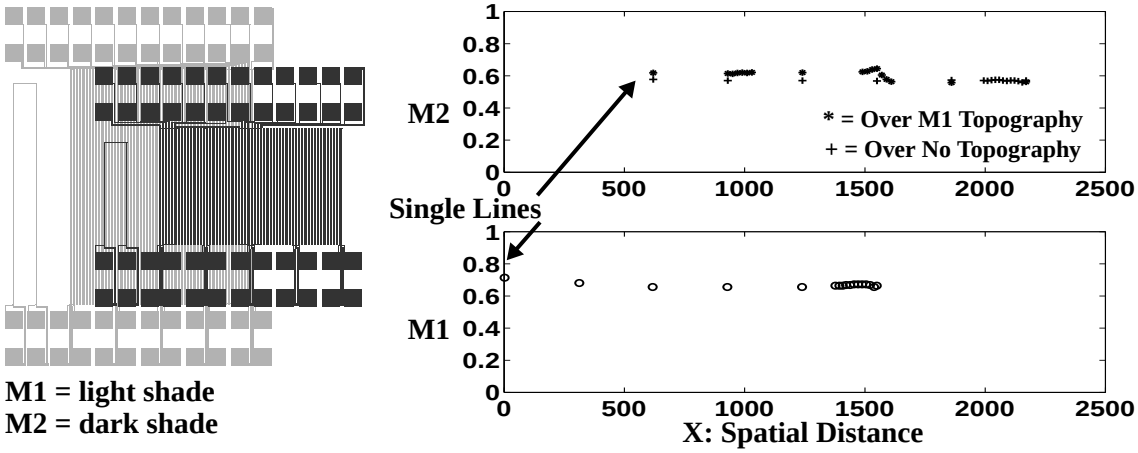


Figure 11. Extracted and Physical Thickness (Lines are shown to distinguish data points)



a. Multi-level Structure (Half Overlap Case)

b. Extracted Copper Thickness (μm) (Original Thickness = 0.8μm)

Figure 12. Multi-level Structure and Extraction Result

C. MULTI-LEVEL AND SPATIAL INFORMATION

The electrical structure described above (e.g. density structure) can be also used to understand spatial variation across a structure and to examine multi-level effects. Figure 12a shows a multi-level structure composed of an electrical test structure on metal 1 and another one on metal 2 from a multi-level mask. The metal 1 structure has an isolated line and an array region. The bottom pads are used to sample data at an equal distance, but the top pads utilize a modified test structure with more finely spaced measurements (or spatial samples) near the right edge of the array. The metal 2 structure is designed similarly except here the top pads sample finely spaced data at both the left edge and the middle of the structure where it is directly over the right edge of the metal 1 structure. Interesting non-uniformities occur near the transition region and this modified test structure design enables us to examine them with our electrical method. Figure 12b shows example extracted copper thickness data using the procedure described. Note that M2 structure suffers more from erosion over the oxide region compared to over the M1 structure region, and it suffers less from erosion when compared to the same M2 structure totally over just oxide on M1.

VI. CONCLUSION AND FUTURE WORK

In this work, we presented an electrical characterization methodology to study the pattern dependent problems of metal dishing and oxide erosion in inlaid metal polishing processes. This methodology is demonstrated by the design of a new electrical test mask, time split experiment and its data, the electrical data extraction, and correlation to physical data. The measured line resistances are converted to physical thicknesses by using the extraction procedure and plotted together with physical data to verify the result. The extracted remaining copper thicknesses are well matched with the physically measured thickness data, and the polishing trends shown for density and polish time dependencies are as expected. This method is being expanded and applied to multi-level polishing characterization and modeling of copper CMP processes.

VII. ACKNOWLEDGMENTS

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