

Fig. 1. Capacitive ILD Thickness Test Structure (left) with Layout Experimental Design Factors (right)

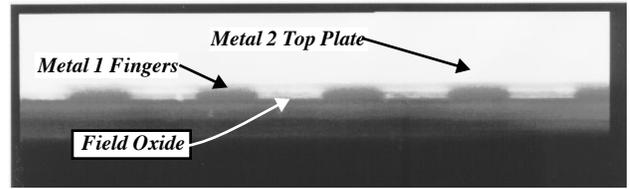


Fig. 5. Verification by SEM Cross-section of Capacitive Test Structure

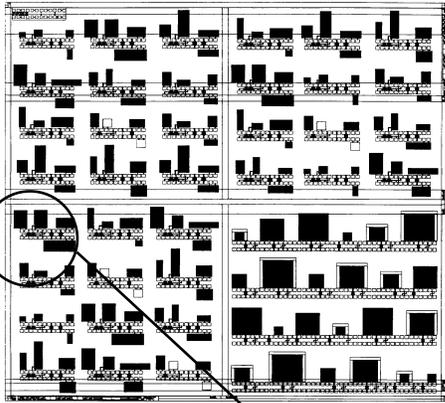


Fig. 2. Die Layout (Area Intensive Structures in Lower Right)

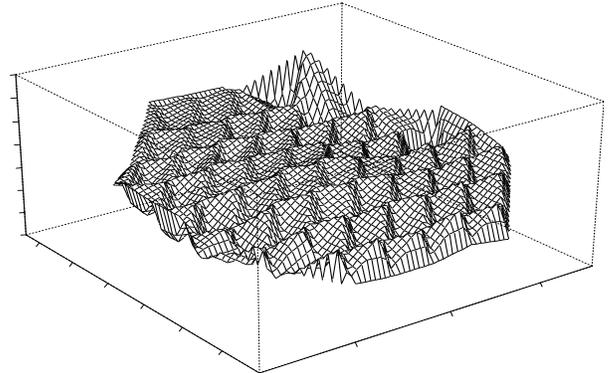


Fig. 6. ILD Thickness (single structure) Across Wafer

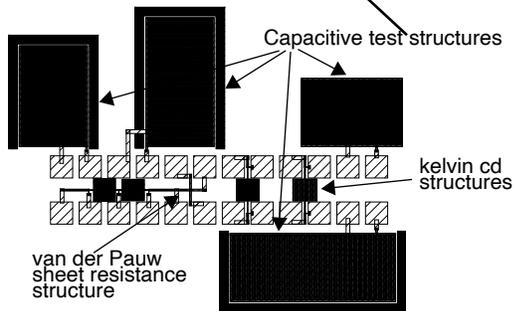


Fig. 3. Subdie Layout: Four Capacitors Near CD Test Structures

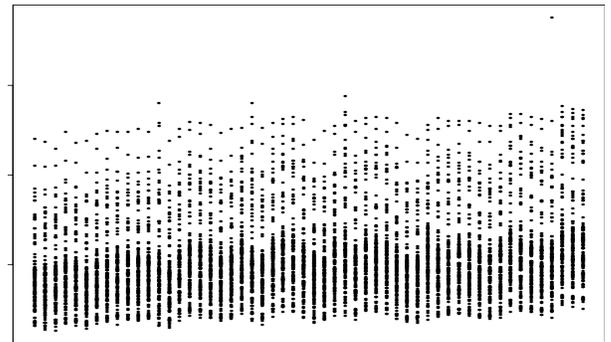


Fig. 7. Die-level Variation (any one die) Larger Than Wafer Trends

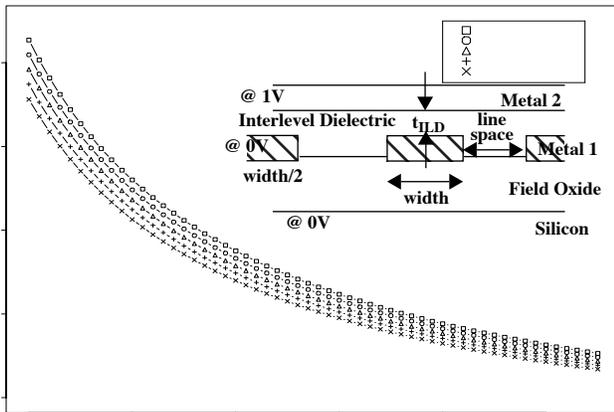


Fig. 4. Raphael Simulation Structure (inset) Used to Generate Capacitance vs. Thickness and Linewidth Interpolation Curve

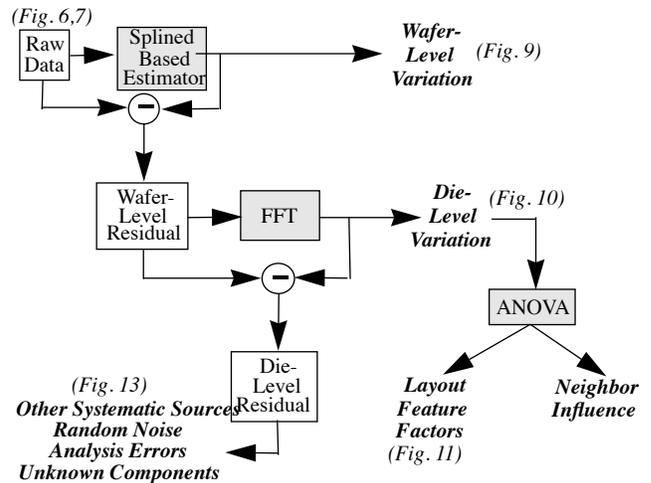


Fig. 8. Variation Decomposition Method

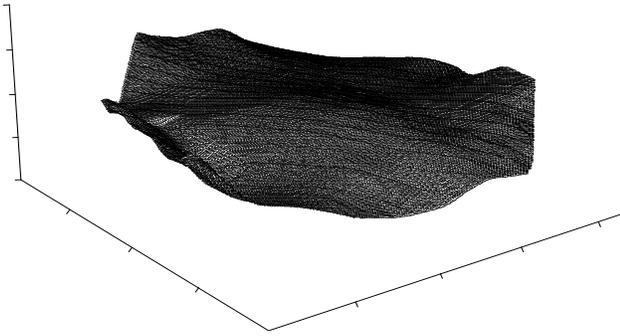


Fig. 9. Systematic Wafer-level Variation extracted via Splined Based Method

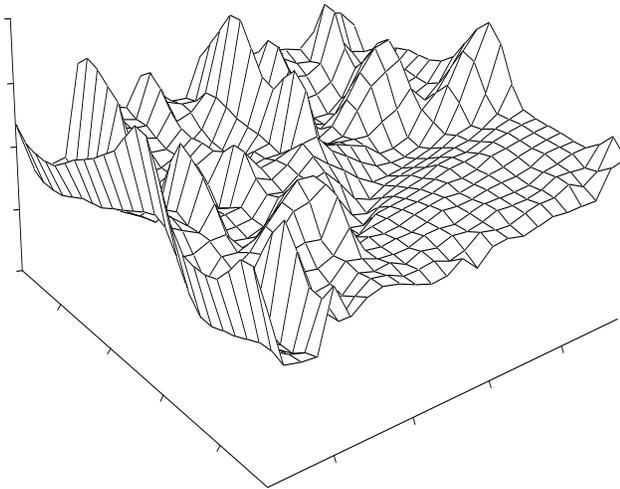


Fig. 10. Systematic Die-level Variation Due to Layout Factors and Neighborhood Effects - Extracted via FFT-based Approach

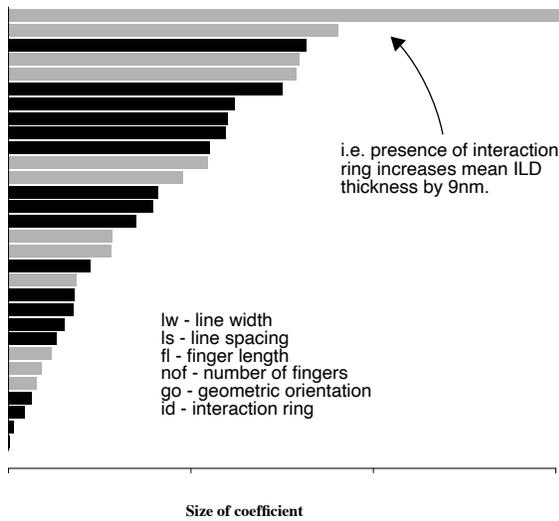
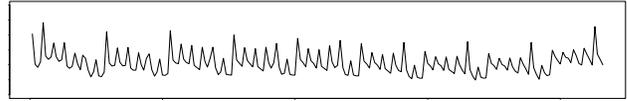


Fig. 11. Layout Factor Contributions to Die-Level Variation from ANOVA

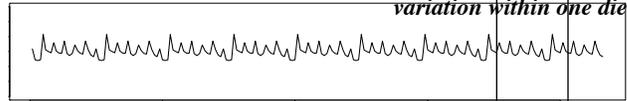
Raw Data



Wafer-level Variation



Die-level Variation



Residual Components

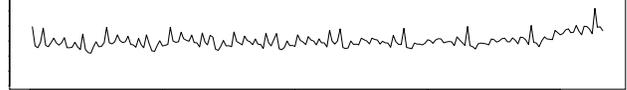


Fig. 12. One-Dimensional Slice Through Wafer Diameter Comparing Contributions to Variation Due to Wafer- and Die-level Variation

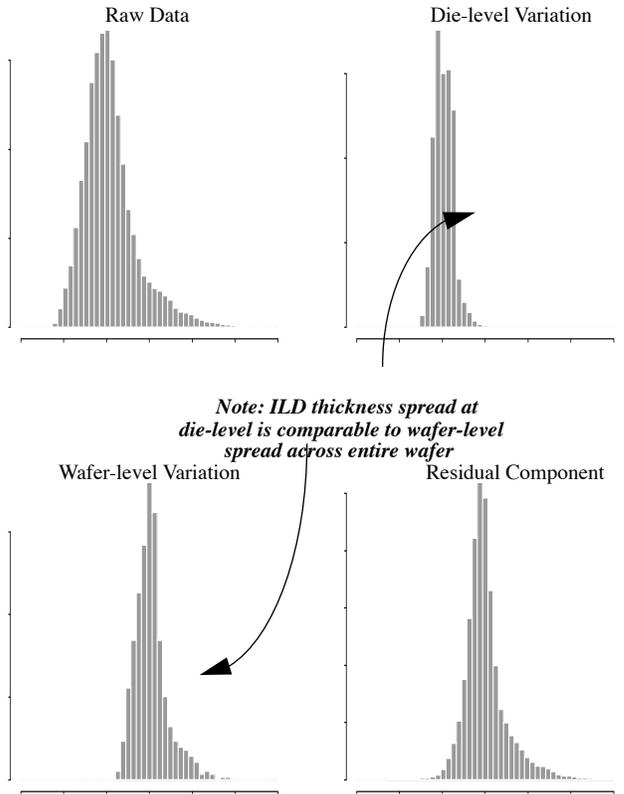


Fig. 13. Histogram Comparing Components of ILD Thickness Variation