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OVERVIEW OF METHODS FOR CHARACTERIZATION OF PATTERN DEPENDENCIES IN COPPER CMP

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ABSTRACT

Copper CMP suffers from well-known but poorly understood dishing, erosion, and other pattern dependent problems. We advocate the systematic study and characterization of these pattern dependencies through the use of electrical and physical test structures and measurements. Three length scales must be recognized: a several mm "planarization length" related to as-deposited copper pattern density, a "transition length" on the order of 100 μm over which erosion profiles change as a function of the local neighborhood, and the feature scale (on the order of 1 μm) dependencies of dishing on line width and erosion on line space. The fundamental structure to explore these dependencies consists of large arrays of lines (~2 mm in size) with a corresponding nearby isolated line, designed as a function of the line width and line space (or metal pattern density and pitch). Electrical versions of these structures enable the extraction of metal line thickness from electrical data. Profilometry provides valuable data on erosion (as well as dishing). Together, these test structures and measurements enable the analysis of trends in dishing and erosion for process optimization, consumable or tool evaluation, and design rule generation. Multilevel polishing effects can also be studied, where the combination of electrical and profilometry data is crucial in order to assemble a complete picture of pattern effects. Future work should examine the interplay between copper and low-k dielectrics, as well as couple to physical models of the CMP process.

I. INTRODUCTION

Pattern dependent issues of dishing in copper metal features and erosion of oxide are a continuing problem in copper CMP [1-9]. Such problems can affect chip performance by introducing variable differences in resistance and capacitance depending on line location within the chip. Pattern interactions also lead to considerable surface non-planarity with consequent manufacturability and process integration difficulties. Figure 1 shows a schematic view of the ideal post-polish profile, in comparison to realistic profiles suffering from dishing and erosion. In this paper, dishing is defined as the recessed height of a copper line compared to the neighboring oxide, and erosion is defined as the difference between the original oxide height and the post-polish oxide height.

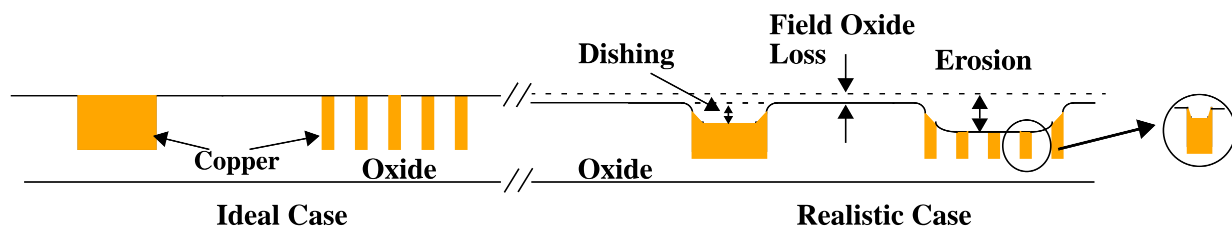

Figure 1. Pattern dependent problems of dishing and erosion in copper CMP.

In this work, we describe a systematic methodology for the characterization of pattern dependent issues and problems in copper CMP. The methodology encompasses test structure design, mask layout, experimental execution, electrical and physical measurement, and data analysis. In Section II, we first consider the major pattern factors that influence dishing and erosion, and discuss the variety of length scales found to be of concern in copper polishing. These length scales and dependencies guide the design of test structures (Section III) and the layout of single layer test masks (Section IV). While most published work has focused on dishing and erosion in a single level of metal, advanced copper interconnect must also address the impact of multiple levels of metallization; multilevel test structures and masks that enable characterization of these effects are described in Section V. The physical and electrical measurements of dish-

ing and erosion are then summarized in Section VI. The analysis and interpretation of these measurements are discussed in Section VII, with an emphasis on extracting key information needed for CMP process comparisons, process optimization, and design rule generation. Finally, Section VIII summarizes and suggests areas for future research.

II. COPPER CMP PATTERN DEPENDENCIES AND LENGTH SCALES

In early studies [1, 2] copper dishing was found to be largely dependent on metal line width, and oxide erosion to be strongly dependent on pattern density. Further work [3, 4, 7] showed that pattern pitch also influences oxide erosion: both the pattern density and pitch, or more fundamentally both density and line space have a first order influence on oxide erosion. The new findings also indicated that dishing is not solely dependent on line width: even with the same line width, significantly different dishing is observed depending on the environment around the line. For example, isolated lines and array lines produce different amounts of dishing even if the line width is the same in both cases [8, 10]. Systematic investigation of dishing and erosion thus requires careful attention to the influence of both line width and line space (or equivalently pattern density and pitch).

Given the observation that the layout neighborhood around a structure of interest has a large influence on dishing and erosion, a key question is over what range or length scale that interaction occurs. In oxide polishing, a single length scale is found to dominate: a "planarization length" on the order of 3-7 mm effectively averages the density of raised topography within that range, determining the relative rates of polish [11]. In copper polishing, on the other hand, three different scales appear to be at work. First, an analogous long-range (e.g. 6 mm in [12]) pattern density dependence appears to be important during the initial planarization of the bulk copper. Second, a relatively sharp and short range transition of approximately 50-200 µm is observed between a field oxide region and the dishing/erosion profile in an array region, or between two different density/pitch array regions [7, 9]. Finally, very short range dependencies on the order of the individual line width or space (0.1 - 10 µm) can substantially accelerate or limit dishing and erosion [9]. The variety of these length scales and dependencies must be accounted for in the design and layout of test structures for copper CMP characterization, as well as in the measurement and analysis of polish data.

III. TEST STRUCTURE DESIGN

In this section we first describe the basic line/array structure used to explore dishing and erosion. We then discuss the key principles and guidelines for structure design and layout to address the length scales discussed above, as well as support physical and electrical measurement of key pattern dependencies. Additional structures for multilevel and other effects are also presented.

A. Line/Array Test Structures

As discussed earlier, dishing and erosion have been found to depend on both line width and line space. To mimic interconnect, arrays of lines and spaces form the fundamental test structure for the study of pattern dependencies (additional structures are discussed later below). Shown in Figure 2a is a test structure that incorporates three regions or elements. First, the "isolated line" on the left gives dishing information for the case where erosion is minimal. Second, a "dummy line" region gives dishing and erosion for a line surrounded by a small region (50 µm wide) containing similar lines. Finally, the "array" region gives information about erosion across a series of lines, as well as dishing within array lines. The entire array structure is relatively large in height (~2000 µm or more), and is separated from the next test structure by substantial oxide spacing of 500 µm to decouple interactions among structures and to give a large field oxide area to serve as a measured surface profile reference point.

This basic structure is also extended with electrical bond pads for electrical testing as shown in Figure 2b. Again, each structure consists of an isolated line, a dummy line region, and a pattern region with electrical bond pads on both the top and bottom of the structure. The "isolated line" consists of two line segments with a bend so that the measurement can be taken from the same set of bottom pads. The array region is made up of serpentine lines providing resistance measurements based on a 4-point Kelvin structure. The use of both top and bottom pads is to increase the number of measurements that can be made on each structure: a spatial sampling along the array is thus possible. Serpentine lines also allow simultaneous resistance measurement on one loop of a line or an array for thickness extraction and continuity test of lines in the density structures.

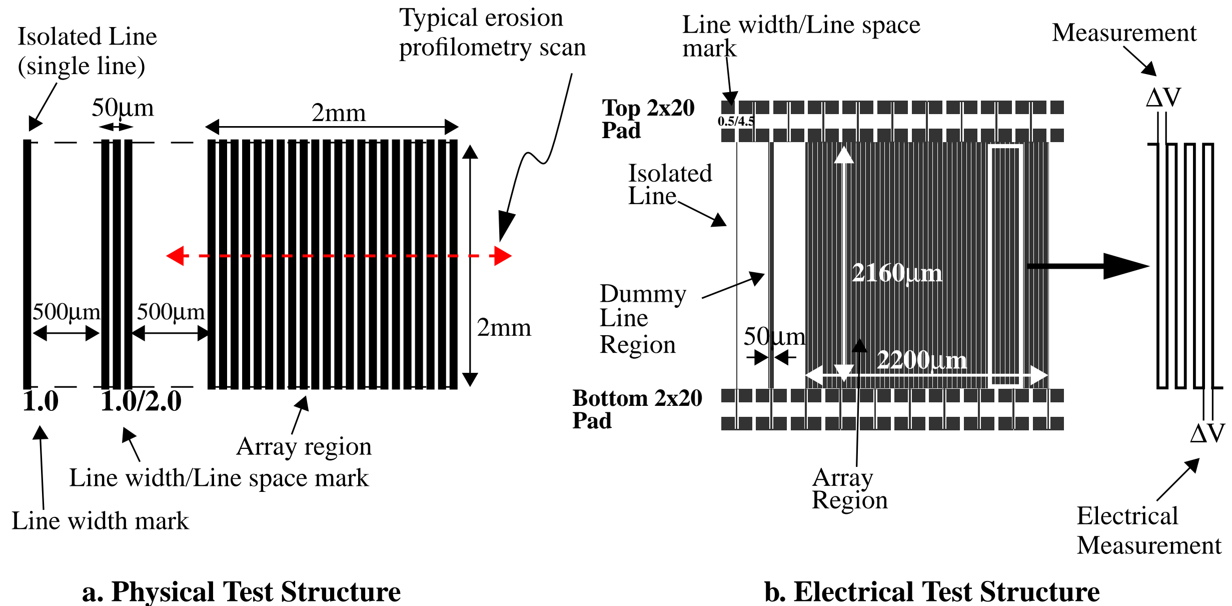

Figure 2. Line and array test structures.

B. Dishing Structure Design Principles

As discussed earlier, dishing depends primarily on line width, but is also be influenced by the nearby environment. Consider the two extremes of the line environment: an isolated line and a line within an array. For a line to be considered "isolated" its polishing behavior should not be influenced by nearby lines. Related studies indicate that oxide spaces with widths greater than 200 µm or so erode relatively little [7, 9, 10], so that separations of 200-300 µm between the isolated line and dummy line or array regions should minimize the impact of erosion on the isolated line. It should be remembered, however, that the bulk copper polish interacts over several mm; by keeping the isolated line relatively near to the corresponding array structure both should experience similar long range averaged pattern densities. Considering the other extreme, dishing within the array will depend on both line width and line space. Typically, the dishing of a line in this case 'sits' on top of the erosion profile which has a rather sharp transition from the field oxide region to the structure region. This length is on the order of 100 µm and thus we want the structure size to be several times larger than this so that a series of lines across the array can be examined.

C. Erosion Structure Design Principles

Erosion depends on both line width and line space, or equivalently on pitch (the sum of line width and line space) and pattern density (ratio of copper line width to pitch). We have found it most useful to design and label the test structures in terms of line width and line space; trends as a function of either sets of factors can be computed and analyzed. For example, "pitch structures" might be a set of structures having a constant density (typically 50%) with varying line width and line space, while "density structures" might be those with a constant pitch and varying density. The test structure size of 2-3 mm is selected to be an appreciable fraction of the bulk copper planarization length, so that a relatively constant effective density region is established within the structure.

D. Additional Structures

In addition to the line/array structures above, other structures are often useful to examine pattern issues in copper CMP. Shown in Figure 3a is a slotting structure designed for a typical bond pad where oxide pillars are inserted into the copper for the purpose of minimizing severe dishing often present with large features. As copper interconnect becomes more fully integrated with low k dielectrics, it will be important to examine capacitances on both the intra-layer and inter-layer levels, and for this purpose a new test structure as shown in Figure 3b has been designed. The structure consists of fingered comb lines on metal 1 for lateral capacitance measurement, and has a solid metal 2 plate for layer to layer capacitance measurement. Though not shown here, additional structures that are being explored include an area structure to examine

polishing dependence on structure size, and alternating pattern factor structures where we alternate pitch or density within the same structure to examine the combined effect.

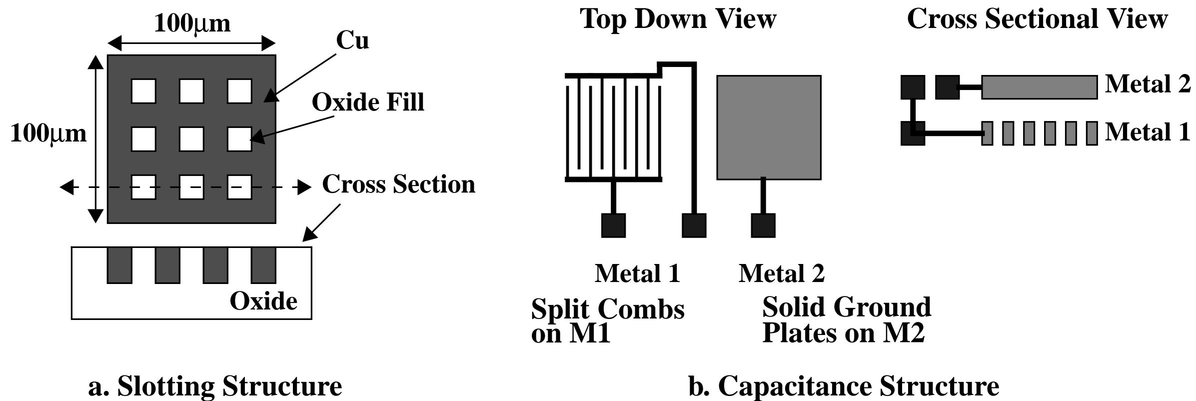

Figure 3. Additional copper CMP test structures.

IV. SINGLE-LAYER MASK DESIGN

The layout of two generations of single-layer copper CMP test masks are shown in Figure 4. At left is a 15 mm x 15 mm chip design showing physical pitch blocks of size 2.5 mm x 3.0 mm at the top, a variety of 3 mm x 3 mm electrically probed density blocks, a number of serpentine and combs to characterize clearing and yield (at 0.35 µm line width and line space), and an assortment of additional structures including control lines, oxide filled pads, and van der Pauw structures. By comparison with a more recent generation mask design at right, a number of lessons learned should be noted. First, the revised chip is larger (20 mm x 20 mm) enabling simplified floor planning and isolation between structures: separations of 500-1000 µm between structures (rather than abutting structures as in the earlier mask) ensure that a "field oxide" reference can be identified for leveling profilometry scans, and shorter scans can be used. Second, the test structures (both physical and electrical) incorporate isolated and dummy regions in close proximity to the corresponding array region, ensuring better correspondence between the observed dishing and erosion. The series of pitch structures at the top are all at fixed pattern density of 50%, and the pitch is varied from 0.7 µm to 200 µm. In the density structures, copper density is varied from 10% to 90% for fixed pitch values of both 3 µm and 5 µm. These density structures can be electrically probed; a variant of the mask in which the probe pads are omitted can also be used. These pitch and density structures, together with assorted additional area, probe pad, and other structures, are effective to characterize dishing and erosion effects in single levels of copper.

V. MULTILEVEL STRUCTURE AND MASK DESIGN

Multilevel CMP effects can be troublesome: topography can accumulate across multiple levels in successive copper patterning and CMP steps. Here we describe extensions to the test structures and mask designs which have been developed to enable study of these effects.

A multilevel test structure is created by using a line/array structure on metal 1 to induce pattern dependent topography in the first level, and then overlaying another line/array structure in metal 2 on top of (nested within) this topography. The dishing and erosion in the metal 2 line/array structure as a function of the underlying topography can then be studied. Shown in Figure 5a is a basic structure which consists of an isolated line (the segments of this line forms a loop with a wide oxide spacing in this case between the lines for better isolation) and an array region; the dummy line regions are not used in this layout. Electrical bond pads and an optional via mask level enable probing of both the metal 1 and metal 2 structures after fabrication (using stacked pads to reach metal 1).

One of the key concerns in multilevel polishing is the ability to fully clear upper level structures residing within recesses created by lower level metal polishing. To study this issue, as well as to map out the transition in polish behavior from one underlying topography to another, a number of "overlap" test structure cases are designed. As shown in Figure 5b, the "half overlap" offsets the metal 2 structure laterally, and Figure 5c shows a "direct overlap" where the metal 2 structure sits fully within the metal 1 topography.

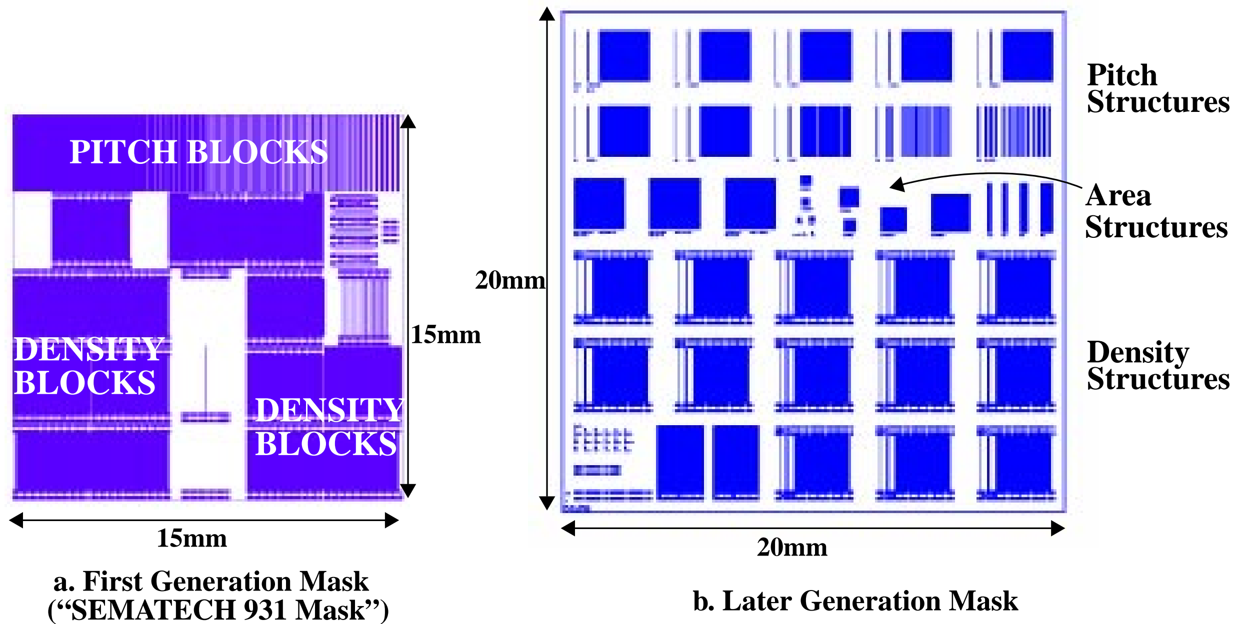

Figure 4. Copper Test Masks (Single Layer)

The more complicated "dual overlap" structure in Figure 5d enables study of the transition from one pattern to another (rather than from one pattern region to field oxide) in metal 1 and the impact of that transition on metal 2 polish. A systematic experimental design in metal 1 and metal density/pitch factors results in the overall mask layout shown in Figure 5e.

Additional minor improvements are made to the metal 1 structures (of size 1250 x 1610 µm) compared to the earlier single level masks. Specifically, a nonuniform spatial sampling of resistances along the line array is used. In each array, the bottom set of pads is used for the measurement of the isolated line as well as to sample from the array of lines at equal distances from the left edge of the array to the right edge. The top set of pads, however, is used to measure lines at finer increments in the transition region near the field oxide. This frequent measurement allows measurement of the pattern topography using electrical data as an alternative to physical surface profile scan data. In a similar fashion, the metal 2 structures (of size 1250 x 800 µm) are spatially sampled to provide more refined information near transitions of interest (depending on the type of overlap).

VI. MEASUREMENT APPROACHES

The characterization methodology described in this paper emphasizes two complementary types of measurements: "physical" measurements (primarily profilometry) and electrical measurements.

A. Profilometry and Optical Measurements

Profilometry and optical film thickness measurements can be performed on both pad-less and electrical structures. Surface profilometry is extremely useful in gathering data about overall topography, but does not directly provide film thickness information. A typical measurement plan for dishing information, referenced to Figure 2a, consists of a short scan made across (perpendicular to) the middle of the isolated line for dishing, as well as a short scan across one or more interior array lines. Erosion data is gathered using a longer scan across the entire array region extending 200-300 µm into the surrounding oxide field. In order to characterize dishing in fine line structures, or to obtain both dishing and erosion along a single long scan, high resolution profilometry is very useful. An example set of profilometry scans is illustrated in Figure 6. Optical (interferometry/ellipsometry) is used to obtain absolute remaining oxide film thicknesses, particularly to reference profilometry scan endpoints in the oxide field regions, and can also be used to measure oxide thickness in large (20 µm or more) oxide spaces. In addition, physical AFM or SEM measurements may also be necessary to confirm and validate physical profile and electrically extracted thicknesses.

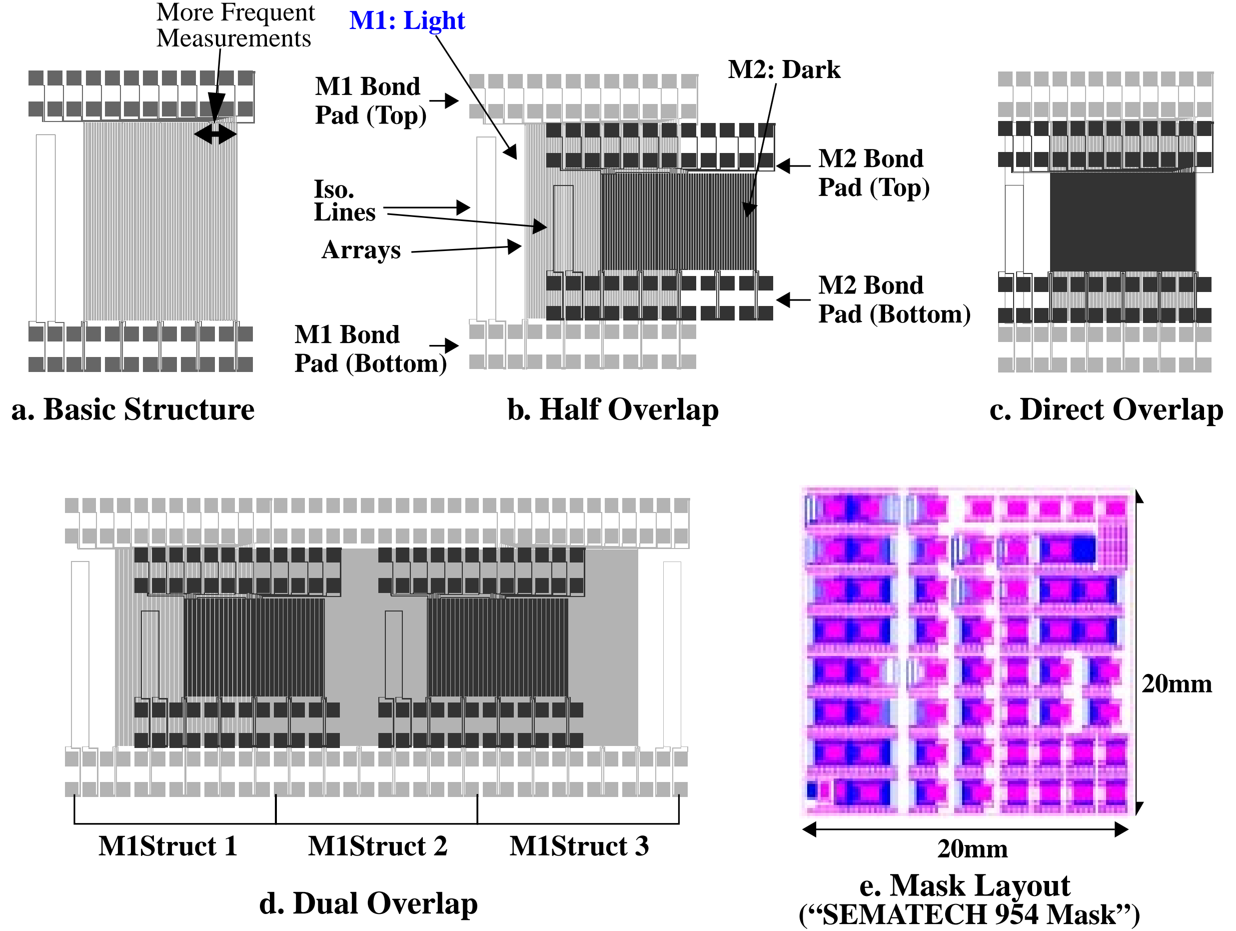

Figure 5. Multilevel mask and test structure layout.

These measurements involve post-polish structures, but it is also important to characterize pre-polish or as-deposited copper profiles: the initial deposition profile can have a strong influence on subsequent polishing behavior. Copper deposition and electroplating is also often pattern dependent, and the test masks in conjunction with pre-polish measurement enable characterization of these dependencies.

B. Electrical Measurements

In addition to surface scans, electrical measurement provides a fast means to gather a complete set of data across all structures, and enables the study of actual electrical characteristics of polished structures. Line resistance is measured and the electrical behavior (such as Rs) can be studied directly, or the resistance could be converted to the corresponding copper line thickness for further analysis. The conversion from resistance R to line thickness (as described in detail in [9]) must account for the barrier or liner thickness T_L as well as any lithographical line width perturbations, to give

$$T_M = \frac{\rho_{Cu}}{R} \times \frac{L}{(W - 2T_L)} + T_L \qquad \text{(Eq. 1)}$$

where W and L are the patterned line width and length, and T_M is the extracted metal line thickness (which includes both copper and liner thickness).

VII. ANALYSIS METHODS

We expect that methods for the analysis of copper dishing and erosion data will evolve with further research. Ultimately, this data should be coupled to a physically based copper CMP model, so that key model parameters can be extracted and the resulting model then applied to arbitrary layouts. Such models

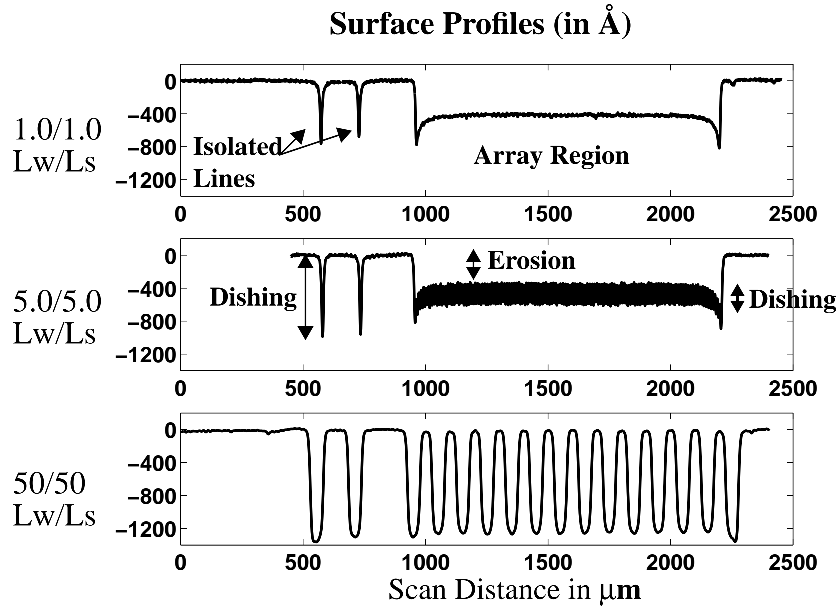

Figure 6. Surface profiles showing dishing and erosion trends in line/array structures.

are still an active area of research. At present, the analysis methodology consists in careful study of the trends and dependencies identified by dishing and erosion data as a function of layout patterns, polish time or recipe, consumable selections, tool design alternatives, or other parameters of interest. In this section we first consider a “minimal” set of data that can provide for rapid evaluation of CMP performance, and then examine more detailed trend analyses. These analyses can be applied to process development and optimization, to guide design rule generation (e.g. min/max rules on density, line width, and line space), as well as dummy fill or slotting strategies.

A. Minimal Pattern Dependent Evaluation

As a minimum set of structures to evaluate dishing, an isolated line and an array line of the same line width are needed for a large feature (e.g. 100 μm line) and a small feature (e.g. 0.35 μm which is the minimum feature on the described single layer masks). These measurements provide “corners” for minimum and maximum dishing for a typical process. For erosion, one needs a low copper density structure (e.g. 10%) for minimum erosion and high density structure (e.g. 90%) for maximum erosion. Thus, a total of four measurements for dishing and two measurements for erosion are necessary, as well as any field oxide thickness measurements needed for field oxide loss. The acquired data then are plotted against the chosen pattern factors and can be compared among different processes or parameter settings. Adding another pitch structure with a feature size between the two extremes for dishing to the measurement plan, as well as a 50% density structure for erosion, provides further detail and trends with a modest increase in the number of data points required.

Figure 6 shows sample data taken on varying pitch structures with the specified line width and line space. Shown on the left of each structure are two isolated lines of the same line width, and the dishing for the isolated cases are all greater than the associated array line. Thus, it is important to indicate whether reported dishing comes from an isolated line or from an array line. Also as expected, the erosion decreases with higher pitch values.

B. Detailed Trend Analysis

Particularly if full electrical probe data is available to complement profilometry, extensive trend analysis can be performed to understand dishing and erosion dependencies. Substantial nonlinearities in these dependencies have been observed, so that such analysis is often needed to gain an understanding of the process. In particular, erosion can be seen to accelerate dramatically for fine line space structures, so that evaluation the available range of pattern sizes is needed. Figure 7 shows an example of the dependence of dishing and erosion on polish time and pitch values using the pitch structures on the 931 mask. The dishing data is for array lines and indicates greater dishing for higher pitch values (thus, higher line width). How-

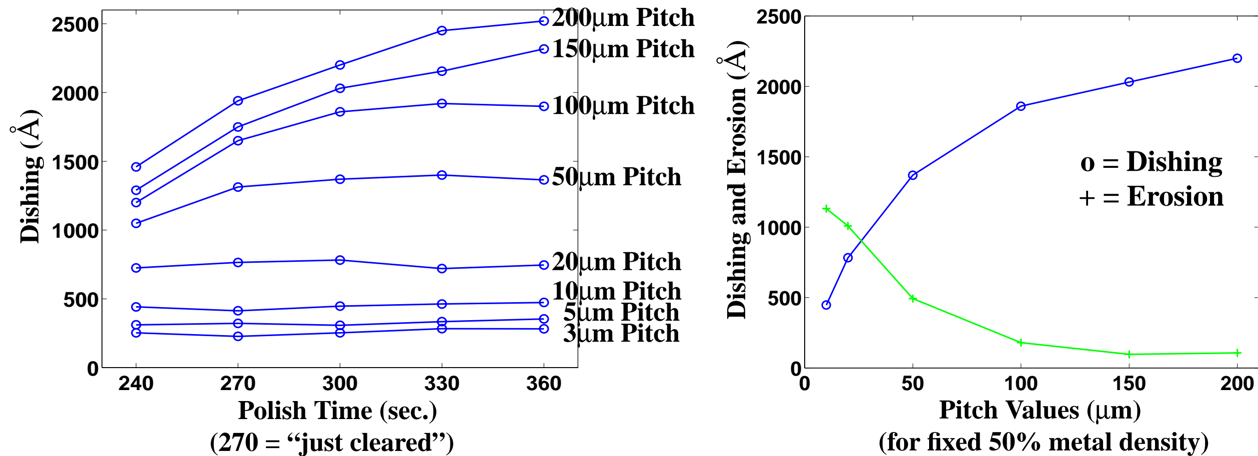

Figure 7. Dishing and erosion dependencies on polish time and pitch.

ever, especially for small pitch structures, the dishing does not increase with more polish time and the larger pitch structures indicate that there is an initial rise of dishing with polish time, which then saturates. Typically, erosion increases with more overpolish, but within an array the dishing has a saturation level (termed steady state dishing) at which the erosion rate and dishing rate are in balance. Figure 7 also shows that erosion becomes very small for pitch values greater than 150-200 µm as previously discussed.

C. Alternative Structures And Analysis

The methods presented in this paper focus on dishing and erosion that arise through the complete copper CMP process (encompassing the copper overburden or bulk removal, the barrier removal, and overpolish stages). Detailed study of the individual stages is of value to better understand the process, and tailored alternative test structures and measurement may be appropriate in these cases. In particular, long range density dependencies in the copper overburden stage are of interest, as density variations within the die can cause different degrees of overpolish across the chip, with resulting differences in dishing and erosion. The extraction of the “planarization length” for this stage may be possible through effective density calculations similar to those used in oxide CMP modeling. However, these extractions are difficult and await a comprehensive and validated copper model. An alternative may be the use of very large feature (several mm) copper trench masks, where down area polishing in large trenches give a more direct indication of planarization length [13]. In these cases, acoustic or other measurements of copper thickness may also be useful. Qualitative comparisons of planarization length scale effects can be made using the single level masks, however, by examining the erosion profiles for high density (e.g. 90%) blocks, where a several mm long “bowl” shape is often observed.

D. Multilevel Analysis

The analysis of multilevel trends must be performed with great care, as multiple effects are at work simultaneously, including the dishing and erosion on metal 1, the oxide deposition profile on top of metal 1 (typically conformal), the as-patterned trench heights (which typically follow the oxide deposition profile), the as-deposited/plated copper topography, and finally the additional dishing and erosion on metal 2. We find that in these studies, the combination of electrically extracted metal line thickness and surface profilometry is indispensable in gaining a picture of the resulting structures.

Consider the electrical and profilometry data shown in Figure 8, together with a schematic cross section at the bottom of that figure. The total metal 2 recess (generated by the metal 1 erosion in combination with additional metal 2 erosion) differs depending on whether the metal 2 line array resides over metal 1 topography or over oxide. Because the bottom location of the patterned metal 2 lines also depends on metal 1 topography, however, we see a reverse line thickness trend (top of Figure 8) where the metal 2 lines over the oxide region are actually thinner than those in the deeper metal 2 recesses. Thus metal 2 erosion profiles alone do not tell the entire story; metal 2 line thicknesses are also needed.

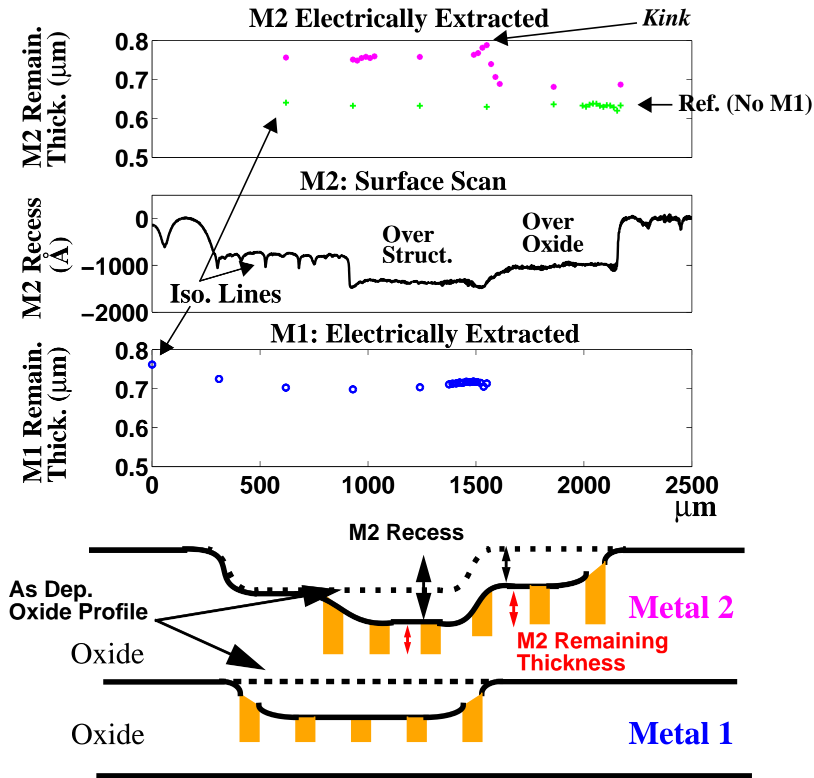

Figure 8. Half overlap structure: profiles and extracted line thicknesses.

We are also interested in multilevel structure impact on copper dishing. Shown in Figure 9 are two plots for a half overlap test structure (similar to the schematic at the bottom of Figure 8, though with substantial dishing into the metal 1 features). At left, we see that the dishing in metal 1 (within large 50/50 structures) largely propagates into the resulting topography of metal 2, where the erosion (in the small 0.5/0.5 structures) on metal 2 reduces the transmitted dishing topography somewhat. In the right of Figure 9, on the other hand, we see the dishing and erosion in metal 2 (for 5/5 structures) over the fine erosion profile on metal 1 (having 1/1 structures) is largely additive. Further analysis and modeling of these and other multilevel effects remains a future challenge.

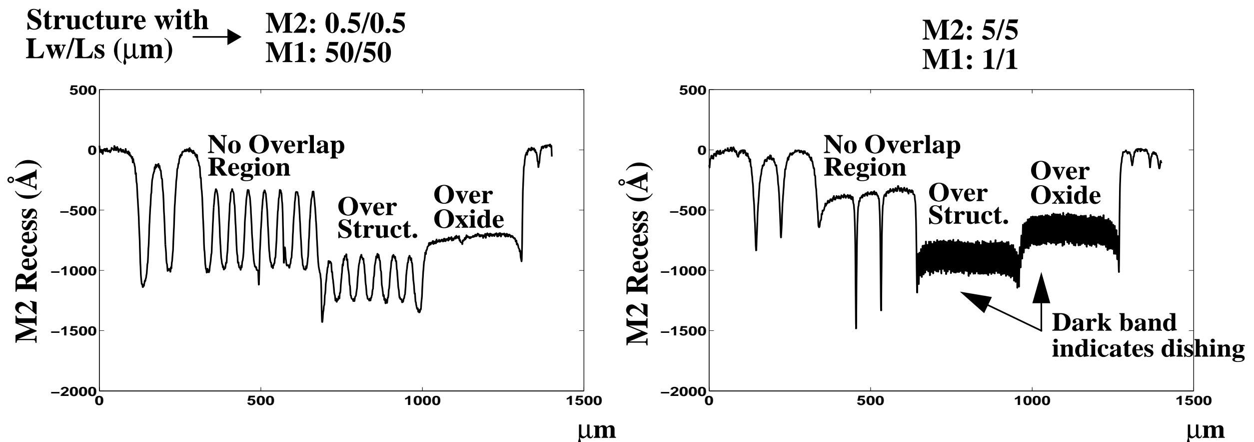

Figure 9. Surface Profiles for Half Overlap: At left we see the metal 1 dishing propagating to metal 2; at right we see the addition of metal 2 dishing to the metal 1 topography.

VIII. SUMMARY AND FUTURE WORK

In this paper, we have presented methods for the characterization of key pattern dependent issues in copper CMP. These methods can be applied to support process development and optimization, and to formulate design rules. We discussed the key length scales of importance in the different stages of polish and how those length scales influence test structure design and data analysis. Physical arrays of lines and spaces, designed as a function of layout parameters, serve as the principle test structure for assessing dishing and erosion. Stacked and overlapped variants of these structures can also provide information on multilevel polishing dependencies. Current and future work includes design of a new multilevel test vehicle for low-k and copper process which adds capacitance test structures so that we can examine lateral and interlayer capacitances and validation of such designs. Copper CMP model development is also needed to capture and generalize the empirical observations enabled by this characterization methodology.

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