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Statistical Metrology - Measurement and Modeling of Variation for Advanced Process Development and Design Rule Generation

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Advanced process technology will require more detailed understanding and tighter control of variation in devices and interconnects. The purpose of statistical metrology is to provide methods to measure and characterize variation, to model systematic and random components of that variation, and to understand the impact of variation on both yield and performance of advanced circuits. Of particular concern are spatial or pattern-dependencies within individual chips; such systematic variation within the chip can have a much larger impact on performance than wafer-level random variation.

Statistical metrology methods will play an important role in the creation of design rules for advanced technologies. For example, a key issue in multilayer interconnect is the uniformity of interlevel dielectric (ILD) thickness within the chip. For the case of ILD thickness, we describe phases of statistical metrology development and application to understanding and modeling thickness variation arising from chemical-mechanical polishing (CMP). These phases include screening experiments including design of test structures and test masks to gather electrical or optical data, techniques for statistical decomposition and analysis of the data, and approaches to calibrating empirical and physical variation models. These models can be integrated with circuit CAD tools to evaluate different process integration or design rule strategies. One focus for the generation of interconnect design rules are guidelines for the use of "dummy fill" or "metal fill" to improve the uniformity of underlying metal density and thus improve the uniformity of oxide thickness within the die. Trade-offs that can be evaluated via statistical metrology include the improvements to uniformity possible versus the effect of increased capacitance due to additional metal.

INTRODUCTION

Statistical metrology is the body of methods for understanding variation in microfabricated structures, devices, and circuits. The goal of this paper is to describe key features of statistical metrology, to review the tools and methods developed to date, and present an application of statistical metrology to advanced technology and design rule development.

A running application example will be used to illustrate the concepts and experience in statistical metrology. In this section, we present the variation problem being addressed, namely the variation of interlevel dielectric (ILD) thickness across the wafer and chip resulting from chemical mechanical polishing (CMP). The progression of our development of statistical metrology concepts and methods will then be presented. These phases are (I) variation assessment, (II) variation modeling, (III) semi-physical model calibration, (IV) circuit impact modeling, and (V) design rule generation. Finally, future work and a summary will be presented.

In essence, this paper serves as a review of the MIT work on statistical metrology. While the references are drawn almost entirely from the MIT research, it is important to note that much work on statistical metrology has been contributed elsewhere (e.g. Spanos et al. (6) and many others) which is not reviewed or addressed in the present paper.

Statistical Metrology

Statistical modelling and optimization have long been a concern in manufacturing. Formal methods for experimental design and optimization, for example, have been developed and presented by Box et al. (1) and Taguchi (2), and application to semiconductor manufacturing by Phadke (3). More recently, these methods are seeing renewed development in "statistical metrology" research. Bartelink introduces statistical metrology in (4), emphasizing the importance of statistical metrology as a "bridge" between manufacturing and design. In (14, 15) an early review of the defining elements of statistical metrology is presented. These include an emphasis on characterization of variation, not only temporal (e.g. lot-to-lot or wafer-to-wafer drift), but also spatial variation (e.g. within-wafer, and particularly within-chip or within-die). A second important defining element is a key goal of statistical metrology: to identify the systematic elements of variation that otherwise must be dealt with as a large "random" component through worst-case or other design methodologies. The intent is to isolate the systematic, repeatable, or deterministic contributions to the variation from sets of deeply confounded measurements. Such variation identification is critical to focus technology devel-

opment or variation reduction efforts, as well as to help in development of device or circuit design rules to minimize or compensate for the variation.

In the next section we describe one process area which is confronted by such intertwined and important variation.

Problem: Oxide Thickness Variation and CMP

The planarization of dielectric layers between multilevel metal layers is critical for present and future interconnect technologies. Variation in ILD thickness remaining after CMP, however, is present at multiple length or time scales. For example, Fig. 1 illustrates example measured wafer-level oxide thickness nonuniformity after CMP, as well as the measured ILD thickness within a sample die. We see that the within-die variation can often be much larger than the wafer-level variation.

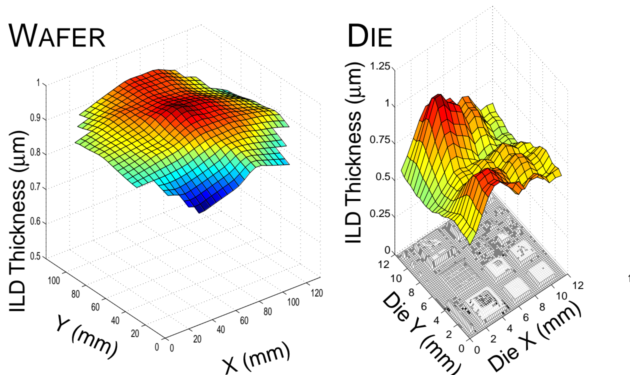


Figure 1: Typical within-wafer and within-die ILD thickness variation. Note that the range within the die is larger than the entire wafer-level trend.

After deposition of oxide over patterned metal lines, local steps are present which one wishes to remove, as illustrated in Fig. 2. While good local planarity can be achieved, different regions across the chip may not polish in a uniform fashion. As also shown in Fig. 2, the reality of oxide CMP is that the process transforms local step height nonuniformity into global nonplanarity: those regions of the chip with higher density of raised topography essentially polish more slowly, so that the final oxide thickness over metal lines in these regions is thicker than that over low density regions.

Progression of Statistical Metrology & ILD Thickness Variation

In order to attack the problem of ILD (oxide) thickness variation described in the previous section, a series of developments has taken place. These are summarized in Fig. 3. In Phase I, variation identification methods were employed. Screening experiments and variation decomposition methods were developed in order to separate and identify the components of oxide thickness variation. Once key elements

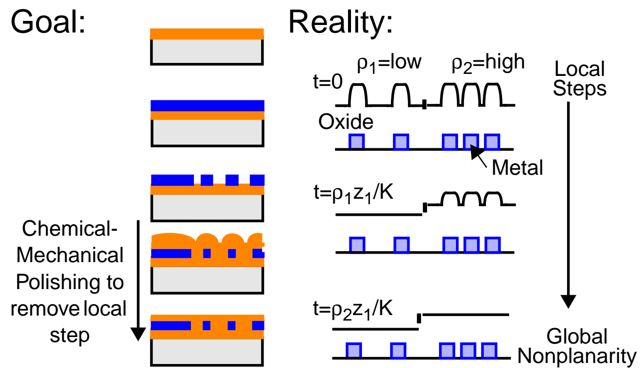


Figure 2: Oxide thickness variation and effect of CMP: the goal (removal of local steps) is shown on the left, while the reality (creation of global non-planarity during step height reduction) is shown on the right.

were identified (i.e. die-level variation), Phase II focused on methods to develop models of that variation. These methods include more focused factor experiments, as well as the generation of empirical models. These experiments result in models with a functional dependency on particular layout practices (e.g. the density, pitch, or area of layout structures). In the oxide CMP case, density was found to be the primary explanatory factor, enabling the development in Phase III of a semi-physical model for oxide polishing. In this phase, a key element is the creation of tightly coupled characterization and calibration methods for extraction of model parameters such as blanket removal rate and planarization length. The resulting CMP model can be applied to predict the topographical variation of oxide thickness across the entire die for a new arbitrary layout. In Phase IV, this CMP variation model is integrated with technology CAD and electronic CAD tools in order to understand the impact of such variation on circuit performance. Finally, in Phase V, trade-offs between structural variation and circuit impact can be evaluated, and design rules guiding the process technology or circuit layout practices generated. In particular, the use of a “dummy” metal fill to reduce the range of density across the chip is considered against the cost of additional capacitance.

In the following sections, each of these five phases will be discussed in more detail and illustrated with historical work in understanding the oxide CMP variation problem.

I. VARIATION IDENTIFICATION

The key purpose of variation identification is to understand what are the potential sources of ILD thickness variation. An experimental approach is undertaken, including determination of (A) measurement strategy and test structures; (B) definition of short flow experiments; and (C) experimental design methods in a search for important lay-

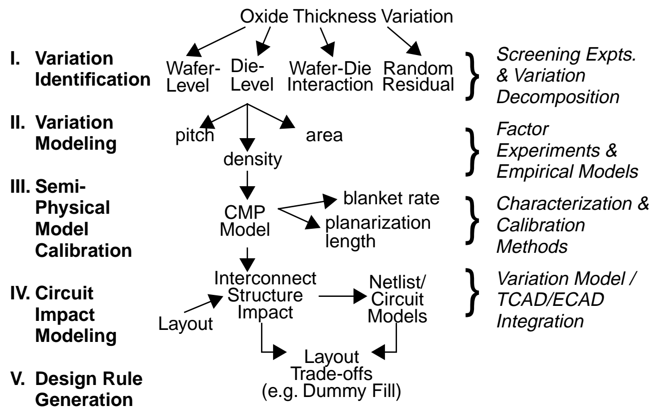


Figure 3: Phases of statistical metrology development as applied to oxide thickness and CMP variation.

out factors.

A. Test Structure Design

Initial investigations of oxide thickness included development of a fingered electrical capacitive test structure, as illustrated in Fig. 4, from which the oxide thickness between two metal layers could be inferred using TCAD tools in conjunction with a large volume of electrical probe measurements (5-8, 11).

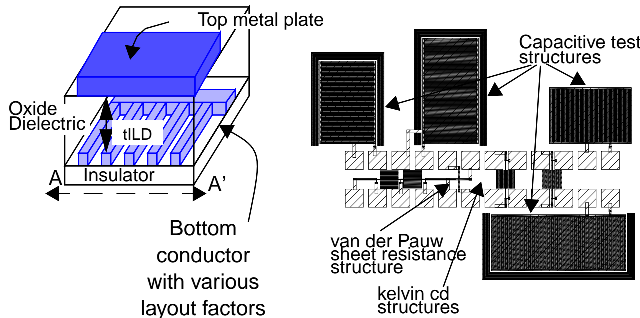


Figure 4: Electrical (capacitive) test structure used to infer the thickness of oxide between metal layers.

B. Short Flow Experiments

The statistical metrology methodology emphasizes short process flows. First, these enable fast feedback and data to be gathered. Second, a shorter flow ensures that the variation being studied is not confounded with that generated by subsequent processing steps. Indeed, substantial care was taken in the test structure of Fig. 4 in order to deconvolve linewidth variation from dielectric thickness variation in the experiment. In later work, optical test masks have been used with the advantage of even shorter process flows and complement the fine line electrical test structures.

C. Design of Experiment Phases

As discussed in (8), three stages of experimental design have been pursued in understanding variation. In the first stage, “screening” experiments seeks to explore a large space of possible layout or process factors that might influence the parameter of interest. Second, “environmental” experiments have been pursued which study how critical parameters depend on factors in a realistic circuit environment (e.g. that of particular product families such as microprocessors, memory, or ASICs). Finally, modeling experiments focus on very specific factors or their interactions, and probe multiple levels of those factors to provide the data needed for empirical models that capture key causal dependencies.

D. Variation Decomposition

Based on electrical or optical measurements taken on many sites within the die, and many or all die on the wafer, a key issue is the assignment of variation in that measure to different sources. In particular, spatial characteristics of the variation can provide substantial insight into the physical causes of the variation. Variation decomposition methods (captured in the “VarDAP” tool) have been developed which successively serve to extract key components from measurement data (16). First, wafer level trends are found, and are themselves often of key concern for process control. The trend is removed from the data, and methods employed to extract the “die-level” variation (that is, the component of variation that is a clear signature of the die layout) using either 2D fourier techniques, or modified analysis of variance approaches (6, 16). This is especially important in order to enable further detailed analysis of the causal feature- or layout-dependent effects on a clean set of data. Third, examination of wafer-die interaction is needed. For example, if the pattern dependencies and wafer level variation are highly coupled, then process control decisions (usually made based on wafer-level objectives) must also be aware of this die-level impact (20). For an example set of raw data (measurements based on the electrical test die (8)), this decomposition is pictured in Fig. 5.

In the case of oxide CMP, we found that the die-level variation is much larger than the wafer level, and is a key cause for concern in the process. ANOVA methods were used to identify both statistically significant effects (care must be taken even here, as spatial location within the die destroys some apparent replications), as well as to estimate the magnitude of effects. A second important aspect of the statistical analysis was the merger of different combinations of the original screening factors into more “natural” or meaningful combinations. For example, the original design was performed in terms of linewidths, line spaces, and number of lines; we found, however, that structure “density” and in some cases “area” provided clearer explanations. At this point, further detailed models of the sources and causes of

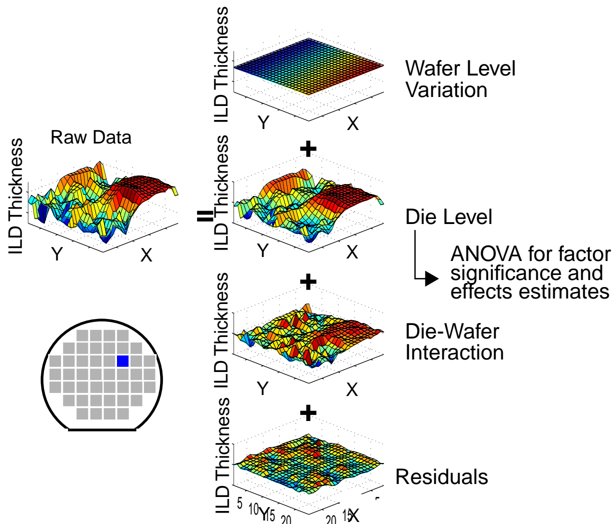


Figure 5: Variation decomposition of ILD thickness.

oxide thickness variation were desired.

II. VARIATION MODELING

As shown in the statistical metrology progression of Fig. 3, the second phase has the goal of more clearly understanding the sources of die-level variation. The key tools are further experimental methods, together with empirical modeling of results (28, 21).

In the case of oxide CMP, a new set of masks were designed which focus on a smaller number of factors (identified in the screening phase), but allowing many more levels of those factors to be explored. A CMP characterization mask set was designed with substantial input from the CMP community, as shown in Fig. 6. In this case, the masks examine: (a) total structure area or size; (b) structure density (e.g. density of patterned lines divided by total area) for a constant structure pitch; (c) structure pitch (sum of linewidth and line space) for a constant 50% density; and (d) structure perimeter over area to explore feature edge effects.

The die-level signatures resulting from oxide polish experiments enable both comparison of the importance of these layout factors in determining polish performance, and effective empirical modeling of these effects. As shown in Fig. 7, quantitative measures of the corresponding layout effects can be estimated. In the case of oxide CMP, we find that pitch and perimeter/area have very little impact, while ILD thickness shows a very strong (and linear) relationship with density. After correction for the density variation, structure area also shows very little clear dependency.

The clear relationship between density and ILD thickness leads directly to the next phase of statistical metrology: development of physical or semi-physical models that can be calibrated to data for analysis of causal variation dependencies.

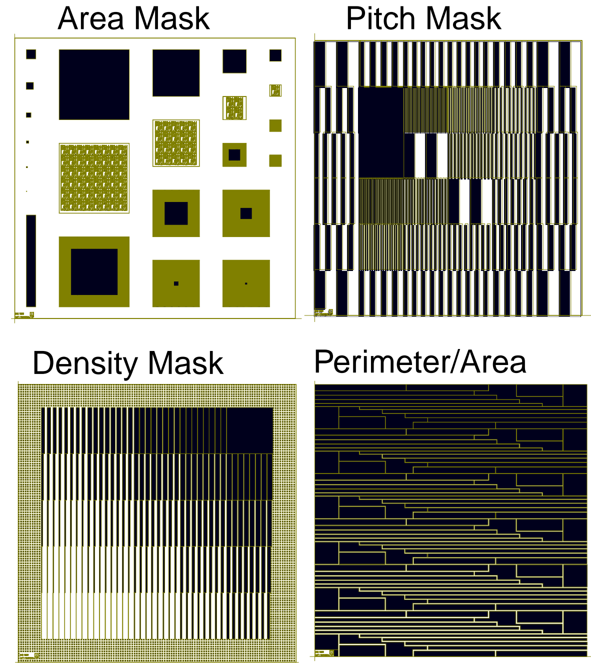


Figure 6: CMP Characterization mask set.

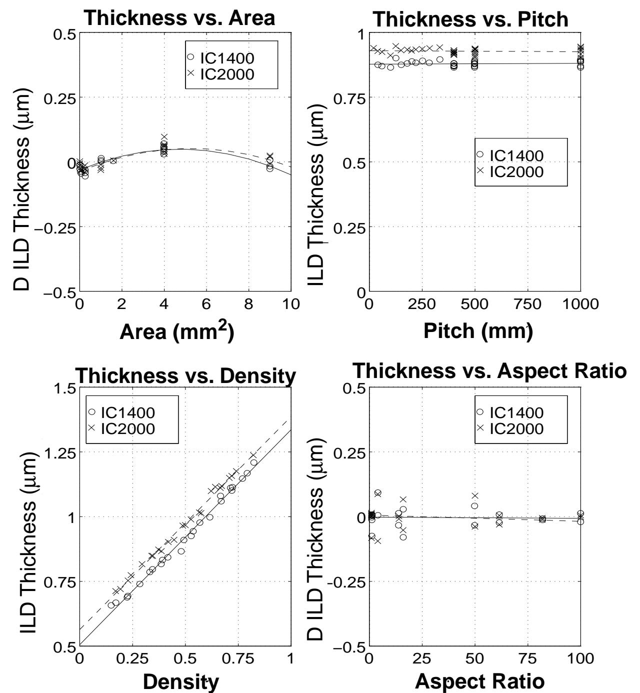


Figure 7: Empirical results from CMP characterization mask set.

III. SEMI-PHYSICAL MODEL CALIBRATION

Based on the characterization mask set, a clear relationship between pattern density and ILD thickness was found. A simple modification to Preston's equation (stating that the bulk removal rate is proportional to the product of pressure and velocity) is used, whereby the overall down-force is distributed only across the "raised" topography (oxide over metal features), leading to a rate dependence on density (18). This relationship is captured as:

$$z = \begin{cases} z_0 - \left(\dfrac{Kt}{\rho_0(x,y)}\right) & Kt < \rho_0 z_1 \\ z_0 - z_1 - Kt + \rho_0(x,y) z_1 & Kt > \rho_0 z_1 \end{cases} \quad \text{(Eq. 1)}$$

where K is the bulk or blanket removal rate, t is the polish time, z_0 is the initial oxide thickness, and z_1 is the initial step height (i.e. the difference in height of oxide between metal features and those over metal features). A key remaining issue, however, is exactly what is meant by "density" (ρ_0 in (Eq. 1) above). As illustrated in Fig. 8, the density is calculated as the raised area to total area in some square (or circular) window determined by a "window size" or planarization length of L. In the case of very fine linewidths, biasing to account for lateral deposition modifies the effective density (17). The size of the window can have a tremendous impact on the effective density calculated at a point on the layout, as well as the range of density found on a chip or along a cut line (such as the B-B' line in Fig. 8). For example, a relatively small window of length 2.5 mm might result in a density range of 57% along BB', while a large window size of 10.0 mm will "average" the local densities much more thoroughly, and result in only a 9% density range across BB'. Through the relationship of (Eq. 1), this density relates directly to the final oxide thickness measured after CMP.

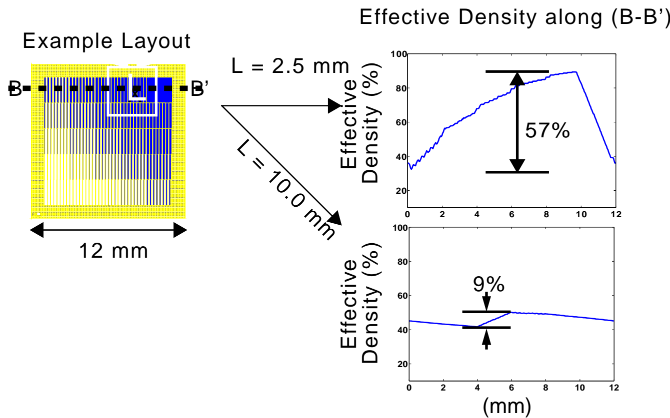


Figure 8: Semi-physical CMP model, illustrating the importance of planarization length (density calculation window size).

The determination of planarization length L, however, cannot as yet be determined based on purely first-principals physical understanding or external measurement of the CMP pad and process. Instead, as part of the third phase of statistical metrology, specific test structures and experimental methods are used to calibrate the model to a given CMP pad and process. As shown in Fig. 9, the planarization length, together with a wafer-level model of blanket polish rate *K(x,y)*, provide the information necessary to predict ILD thickness for any die on a new arbitrary layout (30).

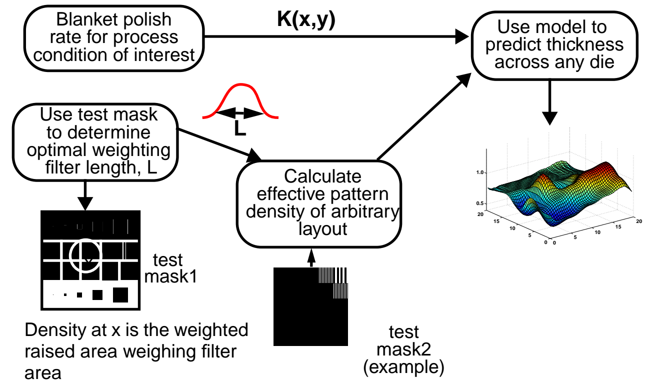


Figure 9: CMP model calibration and use.

Fig. 10 shows an example verifying a calibrated CMP model. In this case, a more sophisticated window shape extraction procedure is employed (30) based on one test mask and experiment. A second, different test mask is shown in Fig. 10, with the corresponding predictions (solid lines) and measurements (circles) for several cut lines across the layout. In particular, cut lines L1 and L2 are drawn along regions of gradual density increase, while L3 is drawn along 4mm blocks of "step density" where the underlying metal pattern density is changed dramatically from one block to the next. Finally, L4 is drawn along constant 50% density blocks where the pitch changes substantially.

Further modeling of the CMP variation can account for the variation of oxide thickness across the wafer (24), as well as other second order polishing effects (26). An important result for multilevel metal modeling is that if the oxide is polished through to "local planarity" then each level of oxide (e.g. between M2 and M3) is affected only by the density on the immediately preceding metal layer; that is, the oxide thicknesses are additive in a multilevel polishing system (25).

IV. CIRCUIT IMPACT MODELING

Based on the statistical calibration and modeling of the previous section, a prediction of the oxide thickness across the chip resulting from CMP is now possible. The fourth key phase of statistical metrology is now undertaken, to under-

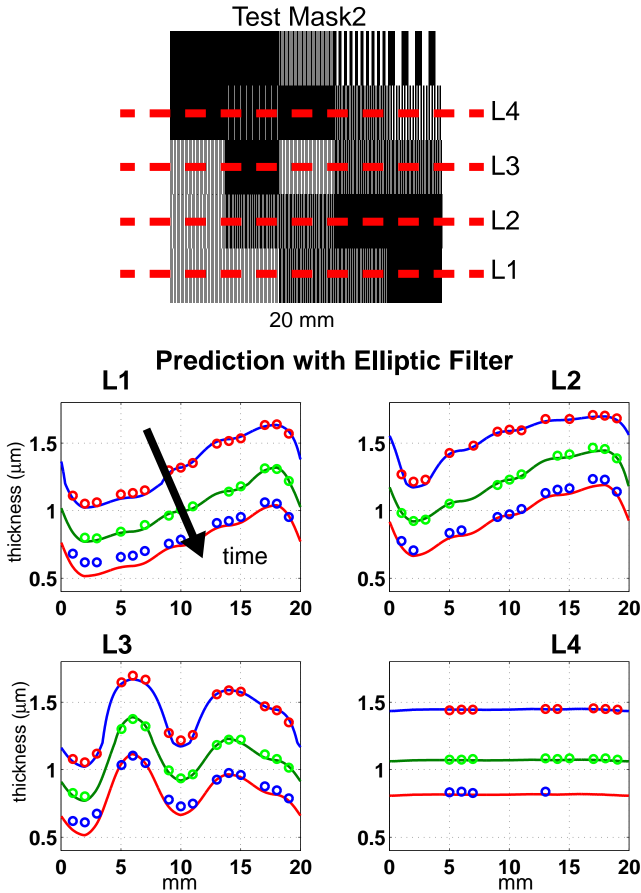
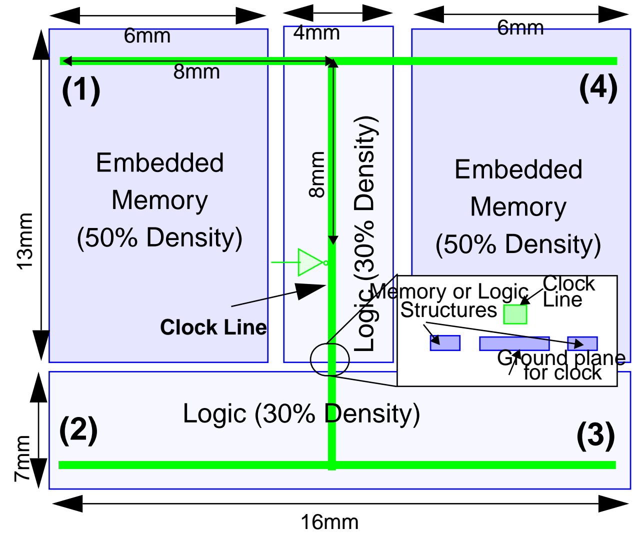


Figure 10: CMP model verification example.



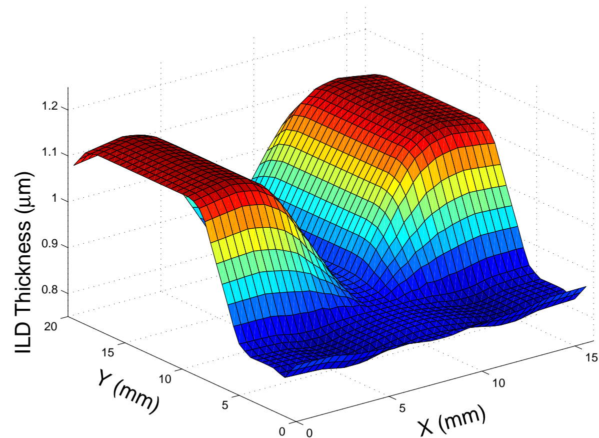


Figure 11: Hypothetical balanced H-bar clock tree floor plan (above); corresponding predicted ILD thickness map (bottom).

stand the impact that such variation may have on circuit performance. In this case, the strategy is to integrate the variation models with process and device simulation (TCAD) tools, as well as with electronic CAD (ECAD) tools in order to evaluate circuit performance (27).

An H-bar balanced clock tree design case study illustrates this approach (27). A hypothetical chip floorplan is shown in Fig. 11, where the goal is to carry the clock signal generated at the center of the chip along the four different paths in such a way that no clock skew results. Unfortunately, the metal clock paths lie over regions of different underlying circuit or metal density. For example, path 1 runs over random logic (with perhaps a 30% density), and then over embedded memory with a higher density of perhaps 50%. Path 3, on the other hand, lies entirely over 30% local density.

As discussed in the earlier sections of this paper, this density difference will result in non-ideal polishing of the interlevel dielectric between the clock line metal layer and the circuit metal layers, as shown in the lower part of Fig. 11. As a result, the ILD thickness along the clock paths, as well as the layer to layer capacitance those paths experience, will be substantially different, as shown in Fig. 12. This disparity can be expected to have an impact on the resulting clock skews; as shown in the lower part of Fig. 12, for example, the difference between the desired and "actual" timing for path 3 is about 17% in this example.

V. VARIATION MINIMIZATION: DESIGN RULE GENERATION

While the fourth phase of statistical metrology discussed above helps to understand the impact of variation, we have not as yet directly addressed a key goal: how does one minimize that variation or its impact? In the fifth phase of Fig. 3, we consider the development of design rules which attack the ILD thickness variation problem.

First, we note that the key variation component is due to the effective density variation or range across the chip. If the density were completely uniform (e.g. 50% everywhere on the chip), then the entire chip would polish at a uniform rate

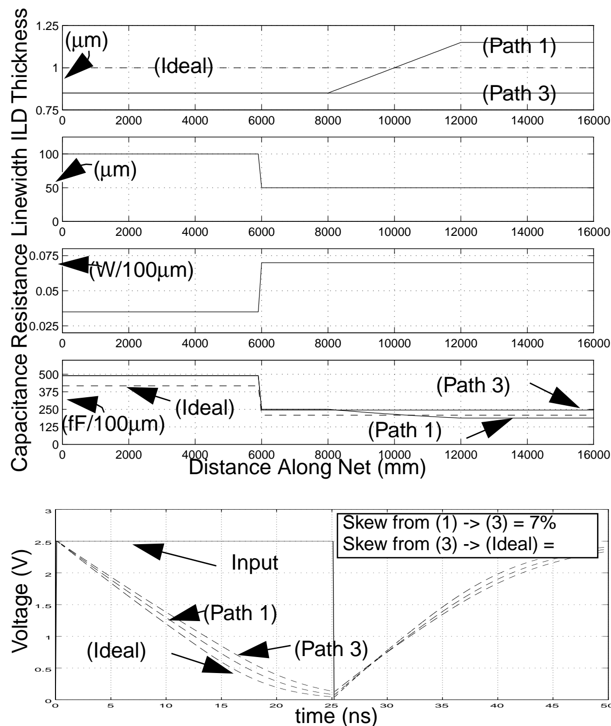


Figure 12: Resulting ILD thickness and capacitance along clock paths (top); resulting clock skews (below).

and a high degree of global planarity could be achieved. As pictured in Fig. 13, however, the range in oxide thickness across the chip directly contributes to the “total indicated range” (TIR) in oxide thickness across the chip:

$$TIR = \Delta z = \Delta\rho \bullet z_1 \quad \text{(Eq. 2)}$$

where $\Delta\rho = (\rho_{max} - \rho_{min})$, and z_1 is the initial step height. For an initial step height of 7500Å and a density range of 80% across the chip, the TIR would be approximated 6000Å. If the density range could be reduced to 33%, then the TIR would be only 2500Å. One approach, then, is to simply mandate to the circuit designer that density may only vary within a relatively narrow range. Of course, CAD tools are needed to efficiently extract the effective density for a given layer, such as those described in Phase III.

One question remains, however: how is one to achieve a target density? One approach with much potential is “dummy fill” of metal lines at the target metal layer. As discussed in (9, 19), different dummy fill practices may be appropriate in different circuit design situations. For example, in the case of high speed microprocessor design, dummy lines (or even plates) may be the most effective; grounding these lines increases the capacitance but to a well-known value. For ASIC design, on the other hand, added capacitance may be undesirable but cross-coupling of lines a concern, so that arrays of floating blocks may be a better choice.

The feasibility of achieving a target density is also limited by pattern dependencies, as well as the availability of

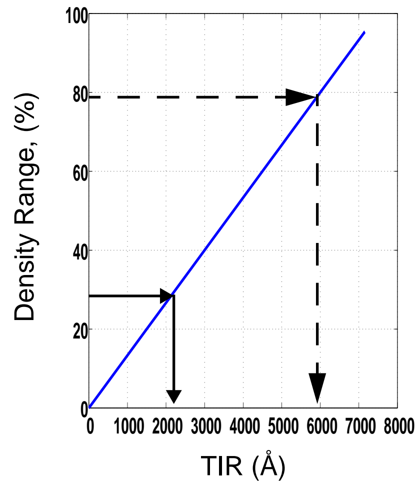


Figure 13: Range of density variation across the chip, and the corresponding total indicated range of oxide thickness across the chip (for initial step height of 7500A).

open space into which the dummy lines (or pedestals) may be placed. As shown in Fig. 14, for example, only linewidths or spaces above particular values my be considered achievable (19). Furthermore, the size of a “buffer distance” between the dummy fill and active lines (which may be substantial in order to minimize the opportunity for lateral capacitive coupling and defect-based shorting) may also impact the achievable density for a given layout.

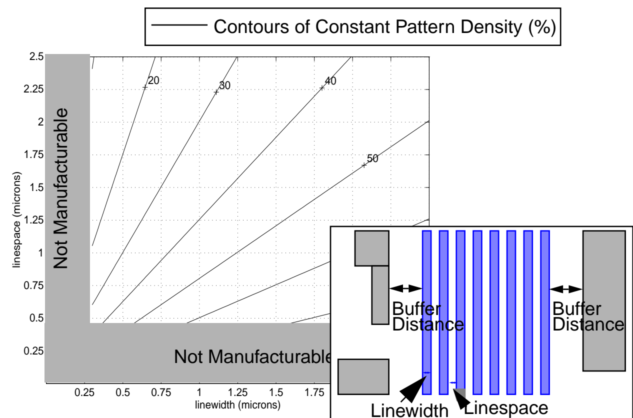


Figure 14: Feasibility of dummy fill densities for dummy line approach.

With even relatively conservative implementations of dummy fill, however, substantial improvements in within-die ILD thickness variation are achievable. For example, in Fig. 15, the distribution of oxide thickness across the die without (left) and with (right) dummy fill structures are shown for a development test chip (9). In this case, the variation was decreased by nearly 20% with the addition of dummy fill.

In creating more clear design rules, however, the tradeoffs between the density and ILD thickness improvement

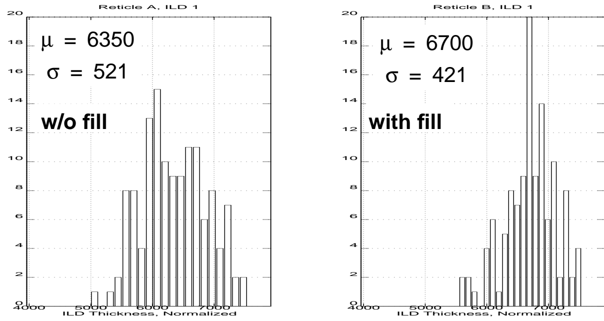


Figure 15: Improvement in ILD thickness distribution observed after addition of dummy fill.

possible with the effect of the added capacitance due to the additional dummy metal must be considered carefully. As shown in Fig. 16, the capacitance for dummy line (or dummy pedestal) can be evaluated for different buffer distances, line widths, and line spaces using capacitance simulation in conjunction with the oxide thickness variation model. A design rule can then be developed based on the trade-off, as shown in Fig. 17. In this case, for example, a 50% density was desired, while essentially 0% increase in the effective capacitance was desired, leading to a particular choice of line space and linewidth for the dummy fill to be added to the layout.

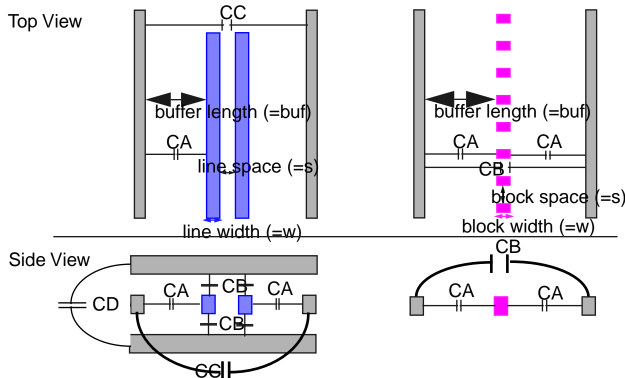


Figure 16: Capacitance impact of added dummy lines. The above capacitance components can be evaluated with capacitance simulation tools.

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SUMMARY AND FUTURE WORK

Spatial variation, particularly that with systematic elements, will become an increasingly important concern in future scaled technologies. Statistical metrology methods are needed to gather data and analyze spatial variation, both to decompose that variation and to model functional dependencies in the variation. Methods are also needed to understand and minimize the impact of such variation.

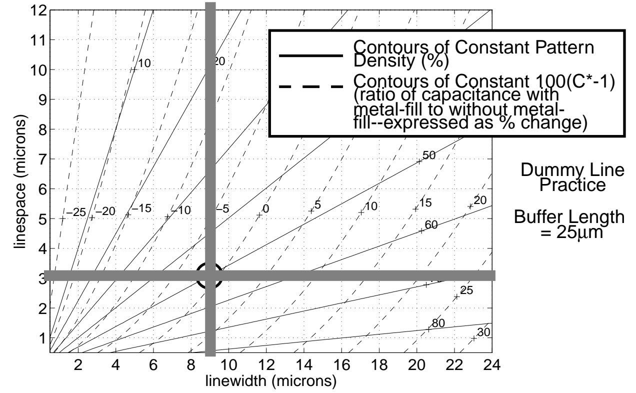

Figure 17: Trade-off between achievable dummy fill densities (solid line), and the net percentage change in capacitance.

In this paper, we have summarized the development and application of a statistical metrology methodology to understanding variation in ILD thickness arising in CMP. The methodology has developed through five successive phases: variation identification, variation modeling, semi-empirical modeling and calibration, circuit impact modeling, and design rule generation.

While the methodology has been developed for the case of oxide CMP, current work is underway to apply and further develop the methods for other pattern and spatial dependent issues in CMP. In particular, shallow trench isolation (STI) also suffers from pattern dependencies (e.g. dishing into large oxide trenches) (31). Even more important for future interconnect technologies, copper damascene suffers from substantial spatial variation, including both dishing into inlaid copper lines, and the erosion of supporting oxide regions in areas of high metal density (32).

We believe that the applications of statistical metrology will be widespread. While we discussed the connection to circuit performance evaluation in this paper, we believe that statistical metrology methods are also extremely powerful in developing and optimizing advanced process technology (e.g. the development of optimal CMP processes (10, 11, 12, 23, 29) or pads that minimize pattern dependencies), as well as in equipment selection and evaluation, and in process control. For example, CMP models are enabling more time and resource efficient processes which minimize the production of waste by-products in CMP. Statistical metrology methods are also seeing application in other process areas, particularly the study of within-chip variations in device and interconnect lines (e.g. MOS channel length) (13, 22).

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