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Using a Statistical Metrology Framework to Identify Systematic and Random Sources of Die- and Wafer-level ILD Thickness Variation in CMP Processes

E. Chang, B. Stine, T. Maung, R. Divecha, D. Boning, J. Chung,
*K. Chang, *G. Ray, *D. Bradbury, *O. S. Nakagawa, *S. Oh, *D. Bartelink
MIT EECS, Cambridge MA 02139 and *Hewlett Packard Co., Palo Alto, CA 94304

ABSTRACT

A statistical metrology framework is used to identify systematic and random sources of interconnect structure (ILD thickness) variation. Electrical and physical measurements, TCAD simulations, design of experiments, signal processing, and statistical analysis are integrated via statistical metrology to deconvolve ILD thickness variation into constituent variation sources. In this way, insight into planarization variation is enabled; for a representative CMP process we find that die-level neighborhood interactions are comparable to die-level feature-dependent effects, and within each die, die-level variation is greater than wafer-level variation. The characterization of variation sources via statistical metrology is critical for improved process control, interconnect simulation, and robust circuit design.

INTRODUCTION

With continued device-scaling, interconnect variation limits system clock frequencies and degrades circuit timing reliability. Chemical-mechanical polishing (CMP) of inter-level dielectrics (ILD) improves planarization but remains hampered by systematic and random ILD thickness variation at the lot, wafer, die, and pattern levels [1,2]. While lot and wafer-level variation has received considerable attention [2], die-level variation continues to increase in importance [3] because of its impact on circuit performance and timing reliability. Previous attempts to study die-level variation have been hampered by the lack of the large amount of statistically significant data needed to model and predict the effects of various factors on ILD thickness variation. Also, die-level variation is convolved with wafer-level variation and must be separated for reliable statistical analysis. The resulting quantification of variation components enables better process development and control (e.g. to minimize wafer scale and pattern-dependent variation), provides realistic data for statistical circuit modeling, and supports the development of tools for layout-dependent prediction of interconnect structures and capacitances.

A novel statistical metrology framework has been developed [4] which integrates electrical and physical measurements, TCAD simulations, design of experiments (DOE), signal processing, and statistical analysis in order to deconvolve the systematic and random sources of parameter variation. For the first time, this methodology has been applied to CMP processes. Statistical metrology is used to generate and extract large amounts of ILD thickness data and present the resulting die- and wafer-level variation for a representative CMP/ILD process. Die-level variation due to layout and other neighborhood dependent factors are found to be comparable, and within the confines of each die, these factors contribute more to variation than do wafer-level trends. To address such issues, improved interconnect, circuit, and layout CAD will utilize statistical metrology.

STATISTICAL METROLOGY TEST STRUCTURE AND EXPERIMENTAL DESIGN

Statistical metrology requires a large number of measurements in order to separate the confounding sources of variation. In the case of CMP, ILD thickness variation is extracted from electrical measurements using a large set of metal-to-metal capacitors. The test structure capacitors have a uniform top plate and a bottom layer (Fig. 1a) consisting of a ladder structure with various combinations of layout factors including finger width and spacing, orientation, finger length, the number of fingers, and the presence of an interaction ring (Fig. 1b). Although useful for verification, optical and cross-sectional SEM characterization are not feasible due to low throughput or measurement limitations (i.e. large optical spot size compared to the layout factors of interest).

Fig. 2 shows the 1.45cm x 1.45cm short-loop test die. Combinations of the six layout factors form a half-fractional factorial experiment resulting in thirty-two unique structures. Each structure is replicated four times per die (eight times per die for the DOE center-point structure). These structures are randomly distributed throughout three of the four die quarters. Large capacitors with fixed underlying width/spacing are located in the fourth die quarter to probe area dependencies often associated with CMP processes [5].

Accurate ILD thickness extraction from electrical measurements requires precise knowledge of the capacitor test structure dimensions. Local estimates of the bottom layer linewidth dimensions are obtainable via resistive measurements [4] using adjacent van der Pauw and Kelvin structures (Fig. 3). To correctly account for critical dimension variation, the Kelvin structures have dummy lines that are spaced similarly to the corresponding capacitors.

The test structures shown in Fig. 2 were fabricated on 6" wafers each containing fifty-four die. A PECVD TEOS layer

was initially deposited to provide electrical isolation. Next, metal 1 (Al:1% Cu with TiN barrier) was deposited and patterned to form the test capacitor bottom electrode. A thick PECVD TEOS forming the ILD was then deposited on top of metal 1 and CMP planarized down to the target dielectric thickness. After tungsten via formation, metal 2 was deposited and patterned to form the top capacitor electrode.

ILD THICKNESS EXTRACTION PROCEDURE

Automated AC (100 kHz) capacitance measurements were performed on each capacitor. Care was taken to account for parasitic components such as pad capacitance. In order to extract the ILD thickness from the capacitance data, look-up tables of capacitance versus ILD thickness were generated for several different canonical 2-D test layout geometries using the capacitance simulation program Raphael (Fig. 4) [6]. To account for fringing fields, the simulated structure has half fingers on the left and right of a center finger (Fig. 4 inset). From the look-up tables, the ILD thickness for a particular capacitance, linewidth, and test structure geometry is determined by linear interpolation. Physical verification of the ILD thickness extraction via electrical measurements has been performed using SEM characterization (Fig. 5).

Fig. 6 shows the extracted ILD thickness (all thickness values are arbitrarily normalized) for one particular type of structure across a typical wafer. Fig. 7 illustrates the ILD thickness versus die location for all the different structures. In both figures, there is clear evidence of local bumpiness due to die-level dependence and of more global variation due to wafer-level sources. The vertical span of ILD thicknesses for each die in Fig. 7 indicates the die-level variation. Fig. 6 suggests that location within a die (even for identical layout factors) can be a major source of ILD thickness variation.

VARIATION COMPONENTS

ILD thickness variation sources can be categorized into die-level, wafer-level, and residual components. Fig. 8 highlights the steps in the analysis procedure to deconvolve the different sources of ILD thickness variation. The wafer-level variation is extracted via a Spline based approach while the die-level variation is extracted using an FFT based algorithm. Detailed description of these and related algorithms are beyond the scope of the present paper.

Fig. 9 depicts the extracted wafer-level variation from wafer M2 of the HP CMP data-set. This wafer-level variation is often low frequency and piece-wise smooth. The shapes and features observed for wafer-level variation are typically caused by process perturbations and are relatively invariant of pattern density or other layout effects. The effect of the wafer edge and flats can be discerned.

Fig. 10 shows the extracted die-level variation, the variation held in common between all die on the wafer, from the HP CMP dataset. Die-level variation is caused by layout feature factors and by neighborhood interactions (e.g. local pattern densities) within the die. The dividing lines between each quad are clearly visible in addition to other locally bumpy features due to individual structures. Finally, analysis of variance (ANOVA) indicates how much of the die-level variation is caused by layout factors or by neighborhood interactions (Fig. 11). The relative size of these terms can be estimated via the ANOVA R^2 value.

The residual component is attributed to Gaussian noise, simulation and analysis errors, other systematic sources of variation, and Poisson occurrences such as stepper flash inconsistencies. While some systematic variation remains in this component, the total range of this variation is substantially less than the original raw data variation and comparable to the other components (Figs. 12, 13). In this way, the original "Gaussian" distribution has been decomposed into systematic components and remaining "random" or un-identified variation.

IMPACT

The methods and techniques presented here can significantly impact both process development and circuit design. Determination of specific variation sources leads to less pattern-sensitive CMP processes. Statistical metrology can be used to understand the effect of different process flows and equipment drift and replacement on both die-level and wafer-level variation. For technology CAD, these techniques represent a prospective means for simulation model development and calibration [8]. These results are also applicable to statistical circuit simulation. From plots similar to Fig. 13, the mean and standard deviation of the wafer-level and die-level variation components can be used as input to Monte-Carlo based circuit simulators in order to predict circuit performance variation caused by layout factors and to predict the expected performance spread across the wafer as a result of wafer-level variation. In this way, designs can be simulated and improved to create variation insensitive designs.

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