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MULTI-LEVEL PATTERN EFFECTS IN COPPER CMP

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ABSTRACT

In this paper, multi-level pattern dependent variations are described and characterized with newly designed test structures. The test vehicle used is a set of two level (metal 1 and metal 2) masks with electrical bond pads connected through vias. Structures on M1 and M2 are combined in various ways to create different M1-M2 overlap cases including direct, half, dual, and cross overlaps. CMP polished surface profiles and electrically determined metal thicknesses show how non-uniformity on M1 (i.e. erosion and dishing) affects M2 polishing behavior. The amount of erosion on M1 as well as what type of overlap is created on M2 both affect M2 polish. We find that the M2 polish creates additional array recess, but the amount of additional recess is smaller when the M2 array resides in a previous M1 array recess region. In addition, the resulting M2 line thickness depends not only on the M2 pattern and polished surface profile, but also on the M1 recess. Thus, determination of final M2 line thickness cannot be inferred from the M2 polish surface profile alone; knowledge of the M1 profile or direct electrical or physical measurement of M2 line thickness as enabled by the proposed test masks is necessary. Understanding and characterization of these multi-level pattern effects is presented for better copper process optimization and integration.

INTRODUCTION

A critical step in copper technology is the use of chemical mechanical polishing (CMP) to remove excess copper outside the desired metal lines and to planarize the surface. In previous work, we have studied the effect of single-level metal patterns on copper dishing and oxide erosion, as such problems affect the manufacturability and performance of a chip by reducing the total Cu thickness which causes a variable increase in copper line resistance. Earlier publications indicate that oxide erosion depends on both density and pitch, and dishing depends primarily on metal line width as well as the environment around the line (e.g. isolated line vs. array of lines). The industry has been gaining understanding on metal 1 polish behavior, and modeling works are in progress [1].

Characterizing and modeling of metal 1 polish with no underlying starting topography is crucial in understanding copper CMP. However, we also need to understand multi-level polishing issues to complete our picture of how copper CMP behaves and how it can be modeled. For this purpose, we have developed a two level mask set dedicated to studying the multi-level pattern effects in polishing of copper. The test masks utilize electrical test structures and the analysis framework presented earlier [2].

MULTI-LEVEL STRUCTURE AND MASK DESCRIPTION

The test vehicle used in this study is a multi-level mask set (metal 1, via, and metal 2) designed with electrical test structures. The goal of the mask set is to understand multi-level effects of M1 on M2 with a wide range of density and pitch structures as shown in Fig. 1. Metal 1 and 2 contain test structures (isolated line and an array of lines) forming

various overlap cases: direct, half, and dual overlaps. In the direct overlap case, the M2 structure is directly over an M1 structure, and in the half overlap case the M2 structure is half-over the M1 structure and half-over the oxide. In the dual overlap case, there are two different M1 structures right next to each other (with different density or layout parameters), and the M2 structure is half-over one M1 and half-over the other M1 structure.

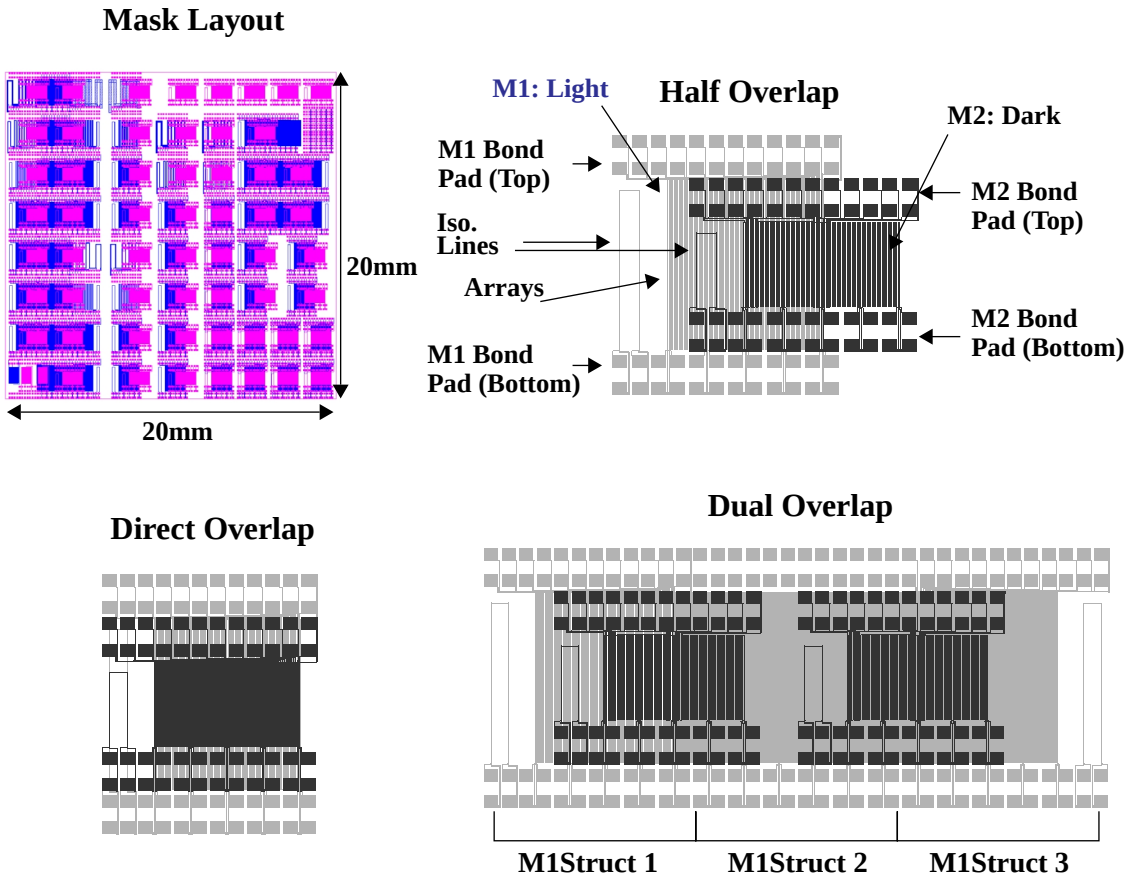

Fig. 1: Mask and Test Structure Layout

All of the M1 and M2 structures (except the middle structure in the dual overlap case) consist of an isolated line and an array of lines forming different pitch and density regions by varying line widths and spaces. The line width of the isolated line is the same as that used in the corresponding array. The array region for each M1 structure is about 1250 x 1610 µm and two sets of bond pads (one at the top and one at the bottom of the array region) are used to measure the line resistance. The bottom set of pads is used for the measurement of the isolated line as well as to sample from the array of lines at equal distances from the left edge of the array to the right edge. The top set of pads are used to measure lines at finer increments near the transition regions.

The array region of the M2 structure is about 1250 x 800 µm and is placed within the M1 structure so that M2's polishing behavior is influenced by M1 non-uniformity only. Each M2 structure has the same bond pad and measurement configuration as the M1 structure. However, the transition regions on M2 are created both by the M2 structure itself as well as by the underlying M1 structure. Thus, depending on the exact overlap case, some M2 structures are measured only at one edge of the array or some are measured both at the edge and center of the array where the M2 center is directly over the edge of M1 structure.

A via layer is used to connect M1 pads to M2 pads, which are placed directly over the M1 pads, so that test structures on M1 could be measured also after M2 polish.

EXPERIMENTAL SETTING

Experiment were carried out at SEMATECH using 8 inch wafers in a single level damascene process where each metal layer (M1, via, and M2) has its own dielectric deposition, pattern and etch, and barrier layer and copper deposition, and polishing. The nominal designed metal thicknesses are 0.8µm for both M1 and M2.

M1 polish is done with a given process for the purpose of creating non-uniform topography and M2 polish is done with different process settings. The surface profiles are measured using a Tencor P10, and electrical testing was done on an HP4062. SEM is also performed to verify data. The copper thickness extraction procedure outlined previously [2] is used to obtain remaining copper thickness from electrical line resistance.

Fig. 2 illustrates the processing sequence in a pictorial format (excluding the via layer for the sake of simplicity). (1) After metal 1 polish, there is a certain amount of oxide recess across a structure region. (2) Because of this starting recess on the metal 1 layer, conformally deposited metal 2 oxide has a similar recess shape as the metal 1 recess. (3) The pattern and etch of the uneven oxide makes the bottom of the copper trenches uneven, and the copper deposition profile is also influenced by the uneven profile shape. (4) After copper deposition and polishing, we are interested in the metal 2 recess and the remaining line thickness in both an overlap region and non-overlap region.

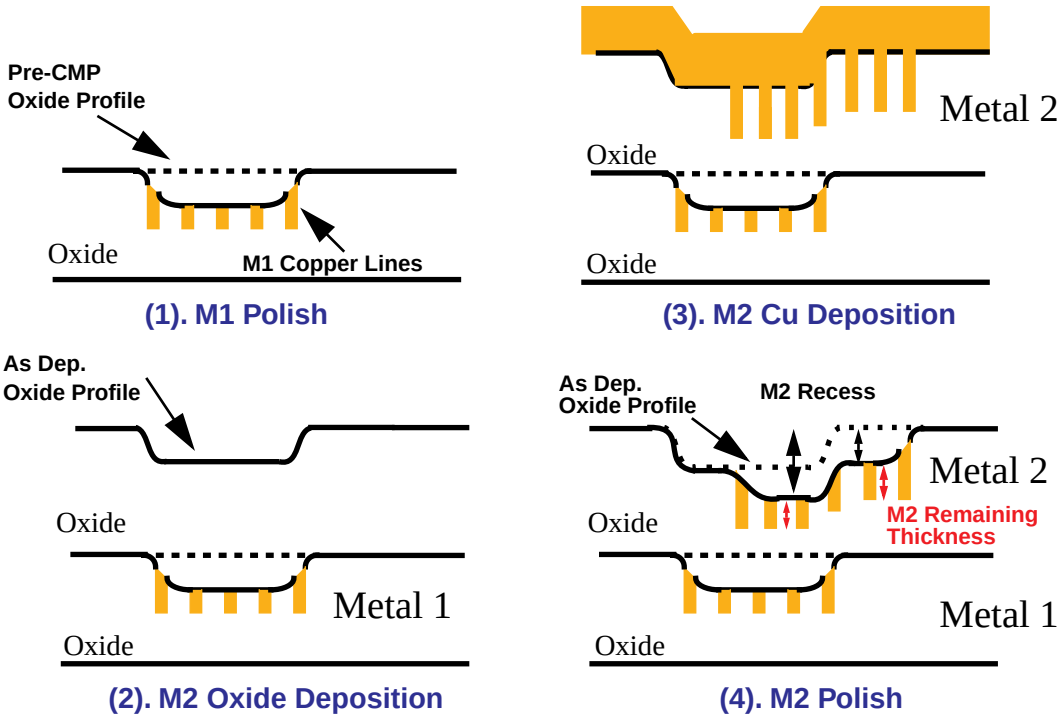

Fig. 2: Multi-level process sequence

EXPERIMENTAL RESULT AND DISCUSSION

Fig. 3 through Fig. 5 show surface scans and electrically extracted remaining Cu thicknesses of M2 and M1 for three different overlap cases with M1-M2 cross sections for one process setting. Note that the cross sectional view and all data plots are aligned vertically. Also shown is a reference “no overlap” M2 structure without any underlying M1 topography (no structure on M1). For the M1 recess, we only show the electrically extracted M1 Cu line thickness because the electrical thicknesses identically follow the shape of the M1 surface recess. In the direct overlap, the whole structure region is

recessed, and the M2 overlap structure shows *more* surface recess than in the reference structure. The electrically extracted Cu thickness profiles follow the surface scan profiles and show higher remaining Cu thickness for the overlap compared to the no overlap case. Although the overlap case has higher amount of recess or erosion, since the starting topography on M1 is also recessed due to M1 erosion, the effective M2 Cu thickness is greater.

In the half overlap, the surface scan shows highest recess in the structure overlap region and slightly less in the oxide overlap region. Because the initial polished M1 profile is not flat due to M1 erosion, electrical thicknesses do not identically follow the surface recess scans. Rather, M2 Cu line thickness depends on both the M1 recess and the M2 polish behavior: it is essential to measure both the line thickness and the surface profile to construct an accurate picture of the resulting M2 structure. Even though the structure overlap region has higher M2 recess, the remaining Cu thickness is greater in that region. Similar behavior is observed in the dual overlap case where the final M2 Cu thickness is greater over the more recessed region on the surface scan. Also seen in both the half and dual overlap cases, the remaining Cu thickness changes from one overlap to another overlap region, more so than the amount of erosion.

In terms of M2 recess vs. M1 recess we want to understand how much recess on M2 is introduced by the amount of M1 recess. The trend is more total recess on M2 as the amount of M1 recess increases. However, the M2 remaining thickness increases even though the surface recess on M2 increases. Thus, the M2 recess is primarily due to the initial starting recess on M1 and that is causing M2 recess to appear greater. Thus, the *additional* recess created during M2 polish is decreased somewhat when the M2 structure already resides with an M1 recessed region. Also note a slight "kink" on M2 remaining thickness right at the transition region for the half and dual overlap cases. This effect is due to the edge effect on M1 where there is slightly more recess (or edge dip) at structure transitions.

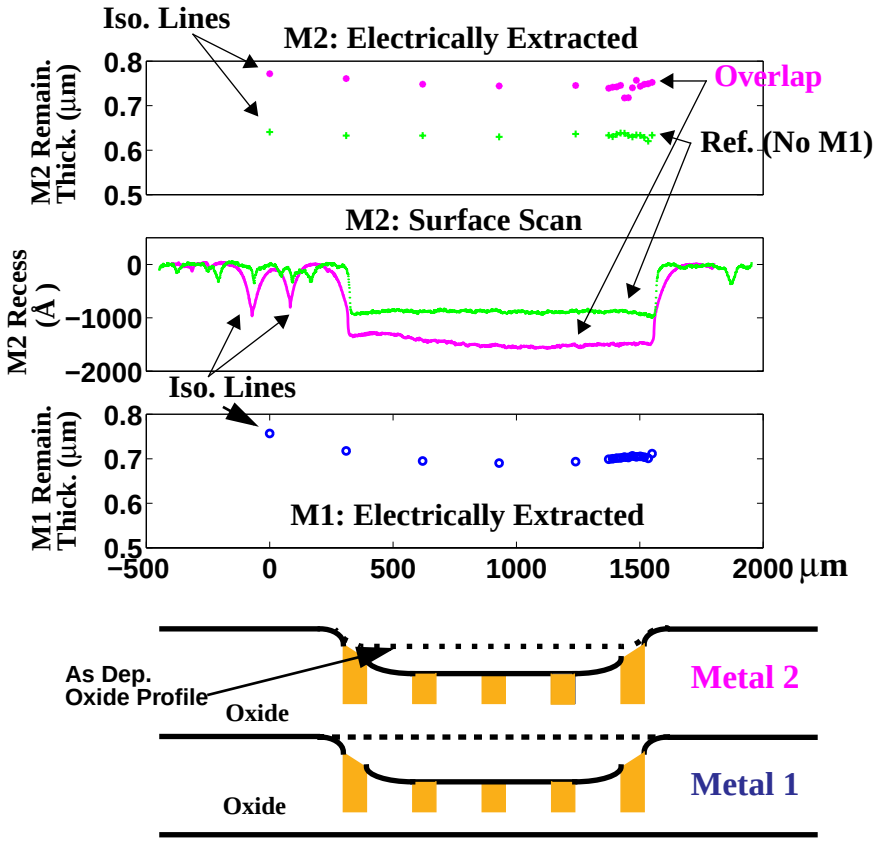

Fig. 3: Direct Overlap: M1 and M2 Surface Profile and Extracted Cu Thickness

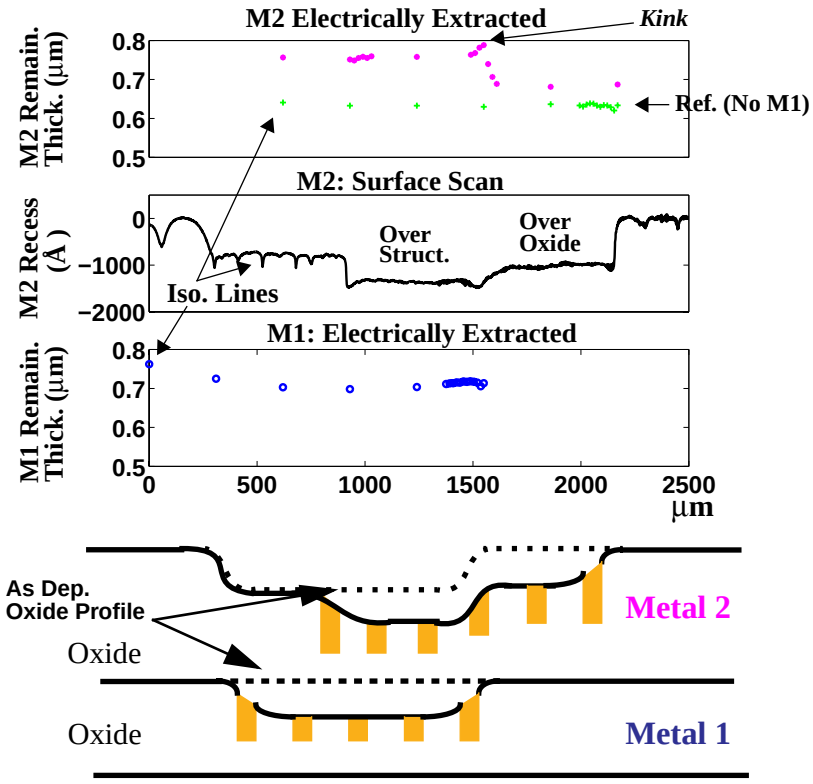

Fig. 4: Half Overlap: M1 and M2 Surface Profile and Extracted Cu Thickness

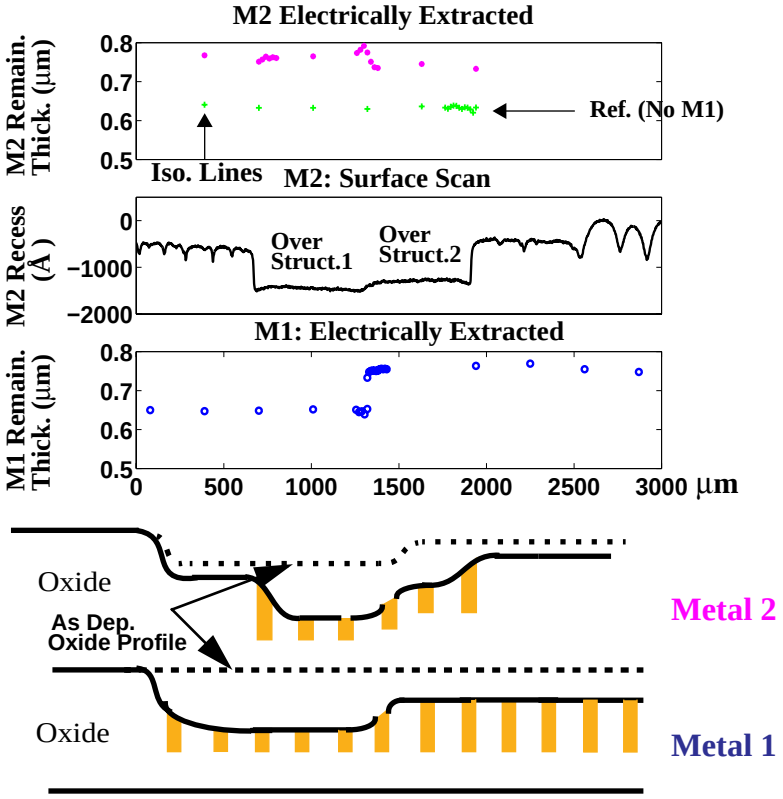

Fig. 5: Dual Overlap: M1 and M2 Surface Profile and Extracted Cu

Shown in Fig. 6 and Fig. 7 are similar thickness and surface plots for a different consumable and process setting. For this process, the difference in the M2 recess and the M2 remaining thickness between the overlap case and no overlap case (reference structure with no M1) is small in contrast to the earlier observation. However, the half overlap case shows higher remaining line thickness in the overlap region compared to the region over metal 1 oxide, and this is consistent with what we observe in the previous case.

We are also interested in multi-level structure impact on Cu dishing. Shown in Fig. 8 are two plots for the half overlap case. The first one shows propagated M1 dishing on M2, and the degree of the propagated dishing is less in the overlap region compared to the no overlap region. The second plot shows propagated M1 recess on M2 with M2 structure dishing where the dishing is constant in both the overlap and no overlap regions. We would expect the dishing to be constant in both regions, assuming dishing occurs on a local length scale and depends primarily on line width.

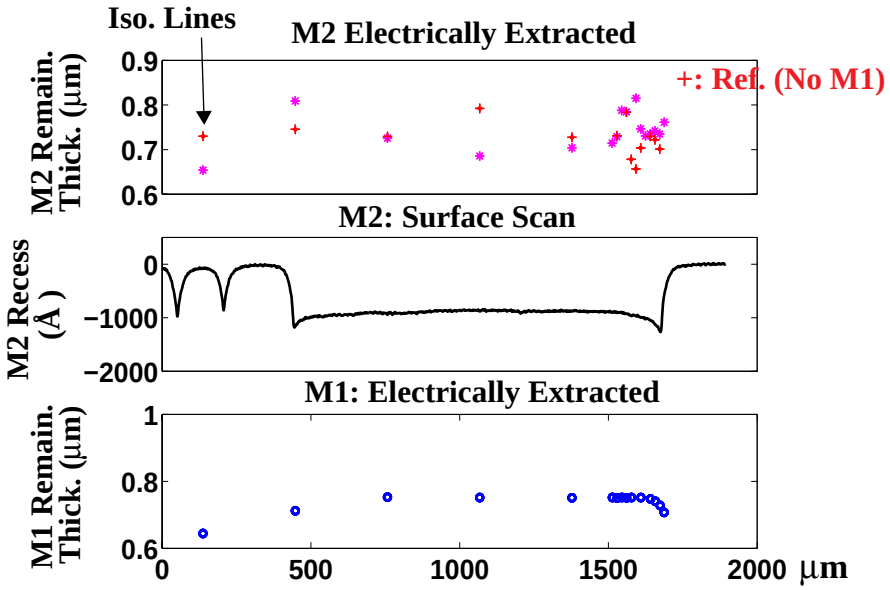

Fig. 6: Direct Overlap: M1 and M2 Surface Profile and Extracted Cu Thickness

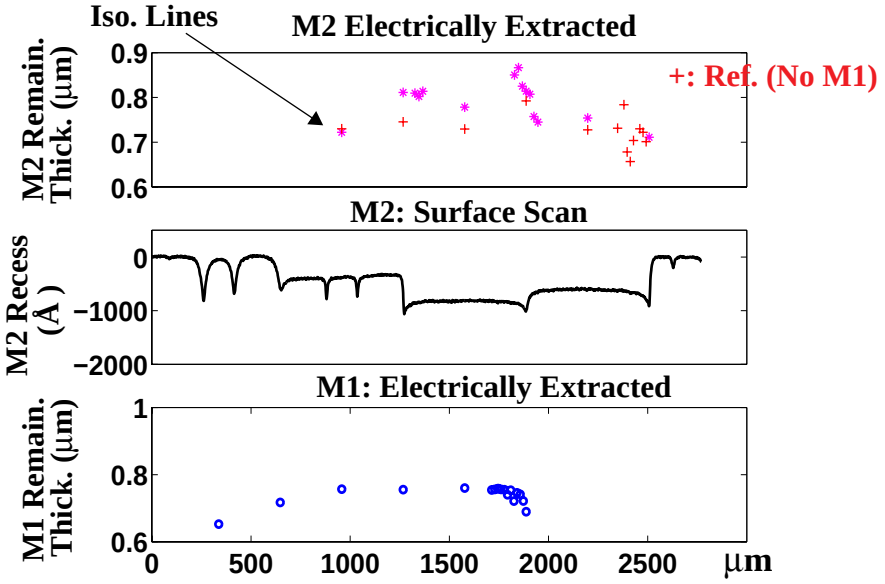

Fig. 7: Half Overlap: M1 and M2 Surface Profile and Extracted Cu Thickness

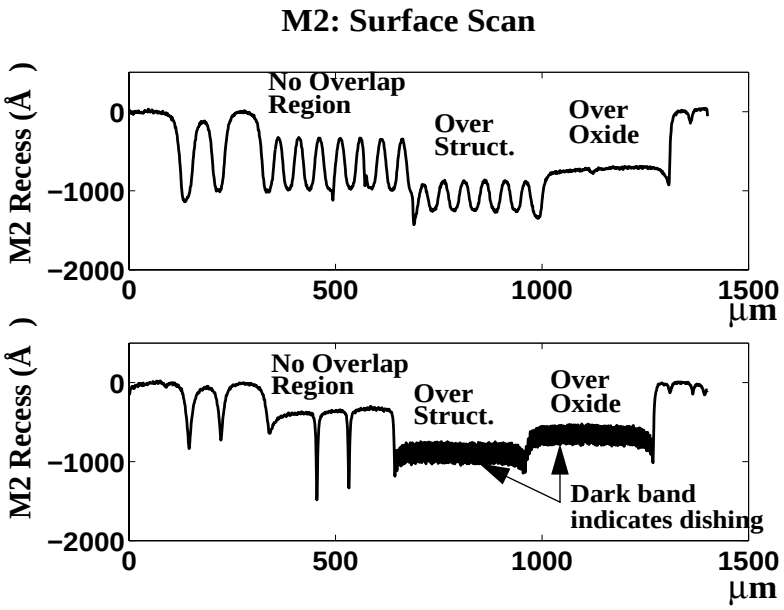

Fig. 8: Surface Profiles for Half Overlap: The first M2 profile indicates M1 dishing shown on M2, and the second profile shows M2 dishing.

CONCLUSION

Characterization and behavior of multi-level pattern effects are presented for better understanding of how layout pattern and initial non-uniform topography influence metal 2 polish. This understanding is crucial for improved process development, optimization, and integration. Further work is in progress to quantify these effects of recess and remaining thickness on M2 and to model these multi-level pattern dependencies.

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REFERENCES

[1] T. Tugbawa, et al., Electrochem. Society Meeting, Hawaii, Oct. 1999.

[2] T. Park, et al., *Proc. CMP-MIC*, Santa Clara, CA, pp. 184-191, Feb. 1999.